



Name : .....

Roll No. : .....

Invigilator's Signature : .....

**CS / M.TECH(VLSI-BL) / SEM-3 / MVET-301A / 2011-12**

**2011**

**LOW POWER VLSI DESIGN**

Time Allotted : 3 Hours

Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

**GROUP – A**

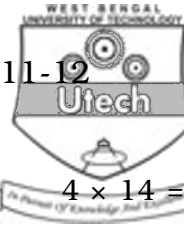
**Answer all the questions**

**7 × 2 = 14**

1. a) What are the properties of VLSI interconnects ?
- b) What is sub-threshold current of MOSFET ?
- c) What do you mean by DIBL in MOS structure ?
- d) What is the advantage of DCSL over other clocked logic families ?
- e) What are the properties of interconnect capacitance of MOS structure ?
- f) Find out the propagation time if the interconnect length is  $0.75 \mu\text{m}$  and relative dielectric constant is 3.
- g) What is quasi-adiabatic circuits ?

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**GROUP – B**

**Answer any four questions**

**4 × 14 = 56**

2. Find out the expression for short circuit power dissipation of an unloaded inverter.
3. Explain the following principles in case of low power design :
  - i) Using the lowest possible supply voltage. 5 + 5 + 4
  - ii) Using parallelism & pipelining.
  - iii) Using smallest geometry.
4. a) Find out the expression for fan out in a domino CMOS circuit.  
b) Find out the expressions for static, dynamic and short circuit power dissipation of a CMOS inverter. 7 + 7
5. a) Explain the power sensitivity method to estimate maximum and minimum average power of CMOS inverter.  
b) What is the significance of transistor reordering in low power design ? 7 + 7
6. a) What is transistor sizing ? Mention its role in low power design.  
b) What is ESTG ? Mention its importance in VLSI design. 7 + 7
7. Write short notes on any *two* of the following : 7 + 7
  - i) Adiabatic inverter
  - ii) Transistor leakage mechanism
  - iii) Estimation of average power in combinational circuit
  - iv) Charge sharing in dynamic CMOS circuits.

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