	Utech
Name:	
Roll No.:	In Agency (1) Executing and Execution
Invigilator's Signature :	

CS/M.Tech (ECE-VLSI)/SEM-2/MVLSI-201/2011 2011

PROCESSOR ARCHITECTURE FOR VLSI

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

(Objective Type Questions)

1. Answer the following questions :

 $5 \times 2 = 10$

- i) "Embedded systems are computers in disguice." Explain it.
- ii) Discuss the general registers organization in ALU design.
- iii) Design a logic circuit taking a $4:1\,$ MUX and some other gates to generate basic logical operations (AND, OR, NOT nad XOR).
- iv) Design a circuit which is taking 4-bit input and increaments its input by 1.
- v) Write a VHDL code which can convert a std_logic input into integer.

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[Turn over

GROUP - B

(Long Answer Type Questions)

Answer any five of the following.



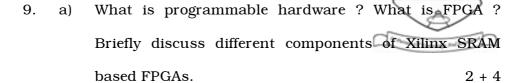
- 2. a) Explain how Modified Harvard architecture is advantageous over Von Neumann architecture.Compare RISC and CISC architectures. 3 + 3
 - b) What are the essential components of an Embedded computer? Briefly describe the components of Embedded computer. 1 + 5
- 3. a) Draw the Direct Buffer Structure using Logic Gates and CMOS. Using VHDL design a 2 : 1 MUX using only tri-state inverters.
 - b) How do you generate a Full adder using only 2:1 MUX in VHDL? 2+4+6
- 4. a) You have two 4-bit numbers. How will you get the product of the two numbers? Describe with proper diagram.
 - b) Design and implement the hardware of 'for' loop. 6 + 6
- 5. a) Discus why CLA adder came into picture in spite of having parallel ripple-carry adder. Draw the block diagram of a 4-bit CLA adder briefly showing each part of it.
 - b) Write down a VHDL code of a 2's complement 4-bit ripple carry adder/subtractor. Then write a VHDL code using structural modelling of 16-bit CLA adder. 2 + 3 + 3 + 4

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- 6. a) What is a logic shifter and what is a arithmetic shifter?

 Design a variable combinational right shifter (both logical & arithmetic)/rotator which can accept 8-bit input and shift from 0 bit to 7-bit.
 - b) Write a behavioral VHDL code of a 4:2 priority encoder. 1+7+4
- 7. a) Design a 16×8 bit single port RAM using VHDL.
 - b) What is Moore and Mealy Machine? Design a 3-bit synchronous counter using FSM approach. 5 + 2 + 5
- 8. a) Suppose we have a data i/p (n bit), now we have to scale this data i/p by a factor 1·646759. Design an architecture of a scale block which can accept this data and does scaling operation by cumulative addition till required scaling as per precision is achieved.
 - b) Design a 4-bit UP loadable Counter whose counting starts from 0100.
 - c) Design and arbitrary counter which can count the sequence 00,01,10,11,10,01,11 in successive clock pulse with unique state representation. 4+4+4

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- b) Make a comparison between different programming technologies of FPGAs. Discuss the operation of EPROM/Flash ROM based programming.
 3 + 3
- 10. a) Implement a 4-input AND gate using CLB of FPGA where each CLB is a 4-input Look-Up-Table (LUT). 4
 - b) Implement the following two functions using Xilinx SRAM LUT based FPGAs :
 - i) $X = A^{l}B^{l} (C + D)$

ii)
$$Y = AK + BK + C^{-1}D^{1}K + AEJL.$$
 5

c) What is PSM ? Briefly discuss the different types of interconnects in FPGA. 1+2