Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(ECE/VLSI)/SEM-2/MVLSI-201/2012

2012

PROCESSOR ARCHITECTURE FOR VLSI DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *seven* questions. 7 × 10 = 70

1. What do you understand by pipelining ? 2

   Define the following terms : 4 × 2

   i) Pipe-stage

   ii) Pipeline machine cycle

   iii) Latency

   iv) Throughput of a pipeline.

2. Define 3 types of pipelining hazards. What could be the easiest common solution ? (3 × 3) + 1

3. y-instructions X---stage : calculate the speed up when pipeline used.

   Define the term "interlocking & forwarding'.

   State the difference between temporal & spatial parallelism.

   4 + 2 + 2 + 2

4. State the difference between static & dynamic branch prediction.

   Describe the difference between control flow and data flow model.

   Describe the difference between super-scalar and VLIW model.

   Describe the difference between Static & Dynamic data flow architecture.

   What is the difference between dual core & dual processor CPU ? 5 ∞ 2

5. What is scoreboard implementation ? Show the implementation of the following example :

```
mul Reg1, Reg3, Reg5

sub Reg2, Reg4, Reg3

div Reg2, Reg1, Reg4

add Reg6, Reg2, Reg3.
```

6. State the Flynn's Classical Taxonomy. Define the advantages & disadvantages of shared & distributed memory. State with example a parallelizable problem & a non-parallelizable problem.

7. Calculate total % of lines saved :

   i) Max Instructions/Line : 5

```
Add R1 R1R1
Add R1 R1R1
Add R1 R1R1
Add R1 R1R1
Add R1 R1R1
```

   ii) Max instructions/Line : 3

```
Add R1  R2 R3
Add R4  R5 R6
Add R7  R8 R9
Add R10 R2 R3
Add R1  R1R1
```

   iii) Max instructions/Line : 2

```
Add R1  R2 R3
Add R4  R5 R6
Add R7  R8 R9
Add R10  R2 R3
Add R1  R1R1
```

   What do you mean by EPIC hardware ? State the advantages of EPIC hardware over general VLIW architecture ?

2 + 2 + 2 + 2 + 2

8. Draw the architecture for PIC 16F877A. State the advantages of PIC micro-controllers over the 8051 micro- controllers. Name one of the compilers used for PIC.

   State how the PWM is obtained in PIC 16F877A. 3 + 3 + 4

9. What do you mean by re-configurable computing ? Define "on the fly re-configurability". What do you understand by IP-cores or customized soft CPU ? How the co-processors and accelerators facilitate the speed-up operation ? What is test bench ? Why do you perform the behavioural simulation ? 1 + 1 + 2 + 3 + 1 + 2