	<u>Utech</u>
Name:	
Roll No.:	(2 Now., V. a., and 1 adm)
Invigilator's Signature :	

CS/M.TECH/ECE(VLSI)/SEM-2/MVLSI-205B/2012 2012

LOW POWER VLSI DESIGN

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

(Multiple Choice Type Questions)

 $1. \quad \hbox{Choose the correct alternatives for the following}:$

 $10 \times 1 = 10$

- (i) The minimum number of MOS transistors are required to design a $2:1\ MUX$ is
 - a) 20

b) 14

c) 6

- d) 4.
- (ii) The output switching activity of a static and uniformly distributed two inputs AND gate is
 - a) $\frac{3}{4}$

b) $\frac{3}{16}$

c) $\frac{1}{4}$

d) 1.

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- (iii) The minimum number of MOS transistors are required to design a 4 inputs dynamic NAND gate is
 - a) 6

b) 8

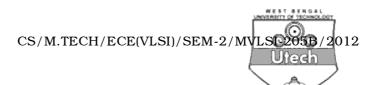
c) 4

- d) 10.
- (iv) Sub-threshold leakage current depends on
 - a) V_{GS}
 - b) V_{DS}
 - c) both V_{GS} and V_{DS}
 - d) independent of V_{GS} and V_{DS} .
- (v) In case of low power memory design, the most important design constraint is
 - a) Switching power
- b) Leakage Power
- c) Short-circuit power
- d) All of these.
- (vi) A Boolean function has m bits output, then the output entropy will be maximum if the probability of each output combination is
 - a) $\frac{1}{m}$

b) $\frac{1}{2}$

c) $\frac{1}{2^m}$

- d) none of these.
- (vii) Switching activity can be reduced using data representation
 - a) Sign magnitude
- b) 1's complement
- c) 2's complement
- d) none of these.
- (viii) Gray coding over binary coding is advantageous because
 - a) Lower switching activity
 - b) Lesser circuit complexity
 - c) Higher speed
 - d) None of these.



- (ix) Advantage of dynamic RAM over static RAM is that
 - a) Needs lesser area
 - b) Lesser power dissipation
 - c) Lesser access time
 - d) Both (a) and (b).
- (x) Delay of a CMOS circuit varies with supply voltages as
 - a) Increases with supply voltage
 - b) Decreases with supply voltage
 - c) Independent of supply voltage
 - d) None of these.

GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

- 2. What do you mean by glitch? How power dissipation due to glitch can be reduced? 1+4
- 3. What is entropy? Explain the method of power estimation using entropy. 1+4
- 4. Explain how voltage scaling helps to reduce power dissipation in a CMOS integrated circuit.
- 5. Describe low power VLSI design techniques at algorithmic level.
- 6. Explain the effect of pin ordering to reduce power dissipation.

GROUP - C

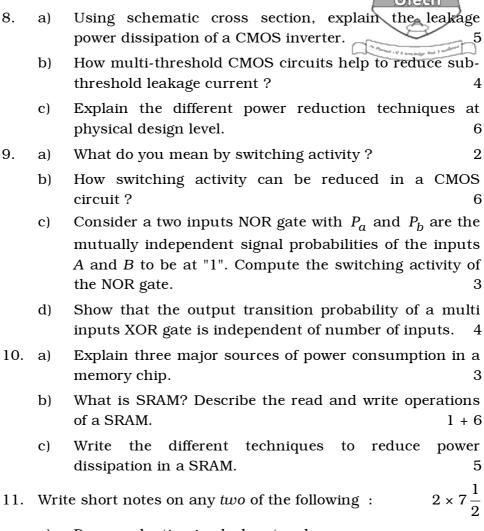
(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

- 7. a) Why low power VLSI design is important?
 - b) Write the expression and degrees of freedom for switching power dissipation in a CMOS VLSI circuit. 4
 - c) Explain how pipelined and parallel architecture help to reduce power dissipation in low power VLSI design. 8

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- a) Power reduction in clock networks
- b) Pre-computation logic for power reduction
- c) Adiabatic Logic Circuits
- d) Variable Threshold CMOS Circuits.