	Utech
Name:	
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Invigilator's Signature :	

## CS/M.Tech (ECE-VLSI)/SEM-2/MVLSI-205B/2011 2011 LOW-POWER VLSI DESIGN

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions.  $5 \times 14 = 70$ 

- 1. Describe the scheme of short channel leakage mechanisms for deep submicron transistors. Elaborate the sub-threshold leakage and gate-oxide leakage mechanisms to its full extent. 4+5+5
- 2. Write the key principles of Low Power Design. Discuss the power dissipation in CMOS inverter. Obtain expressions for short-circuit and dynamic power dissipation of a CMOS inverter. 4+3+4+3

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- 3. Write short notes on any *two* of the following:
  - a) Multiple threshold voltage technique for leakage power reduction.
  - b) Low power adders half adder and full adder.
  - c) Flash memory.
- 4. What are the sources of software power dissipation? Give a vivid idea about optimization of software for low power to estimate the power dissipation at gate level and architecture level. What is bus switching activity? Give an instructional level power analysis. 3 + 5 + 3 + 3
- Describe the source of Static Random Access Memory
  ( SRAM ) power. Discuss the development of low power circuit techniques including capacitance reduction,
  A.C. current reduction, pulse operation and leakage current reduction. Highlight the aspects of future trend and development of SRAM.

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- 6. Discuss the multiple and dynamic supply voltage design to reduce the power consumption in a system. What is power supply network? State the effect of varying the clock speed. What is gated clocking? 4+3+2+2+3
- 7. What do you mean by low power multiplier? Discuss various types of multiplier architectures using flow-chart. What is Braun multiplier? Estimate its architecture, performance and speed consideration. 2+6+1+2+1+2
- 8. Define the term "low power ROM technology". What are the sources of power dissipation? State the effective means to realize power saving in VLSI systems by considering voltage scaling. Describe erasable programmable ROM ( EPROM ) and electrically erasable programmable ROM ( EEROM ). 2+2+2+4+4

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