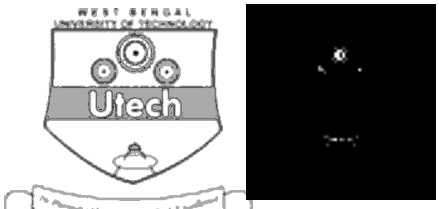
CS/M.Tech(VLSI & MCS)/SEM-2/MVM-201/09
ARCHITECTURAL DESIGN OF VLSI SYSTEM (SEMESTER - 2)



1. ..... *Signature of Invigilator*

2. ..... *Signature of the Officer-in-Charge*

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

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CS/M.Tech(VLSI & MCS)/SEM-2/MVM-201/09

ENGINEERING & MANAGEMENT EXAMINATIONS, JULY – 2009

ARCHITECTURAL DESIGN OF VLSI SYSTEM (SEMESTER - 2)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. You have to answer the questions in the space provided marked 'Answer Sheet'. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

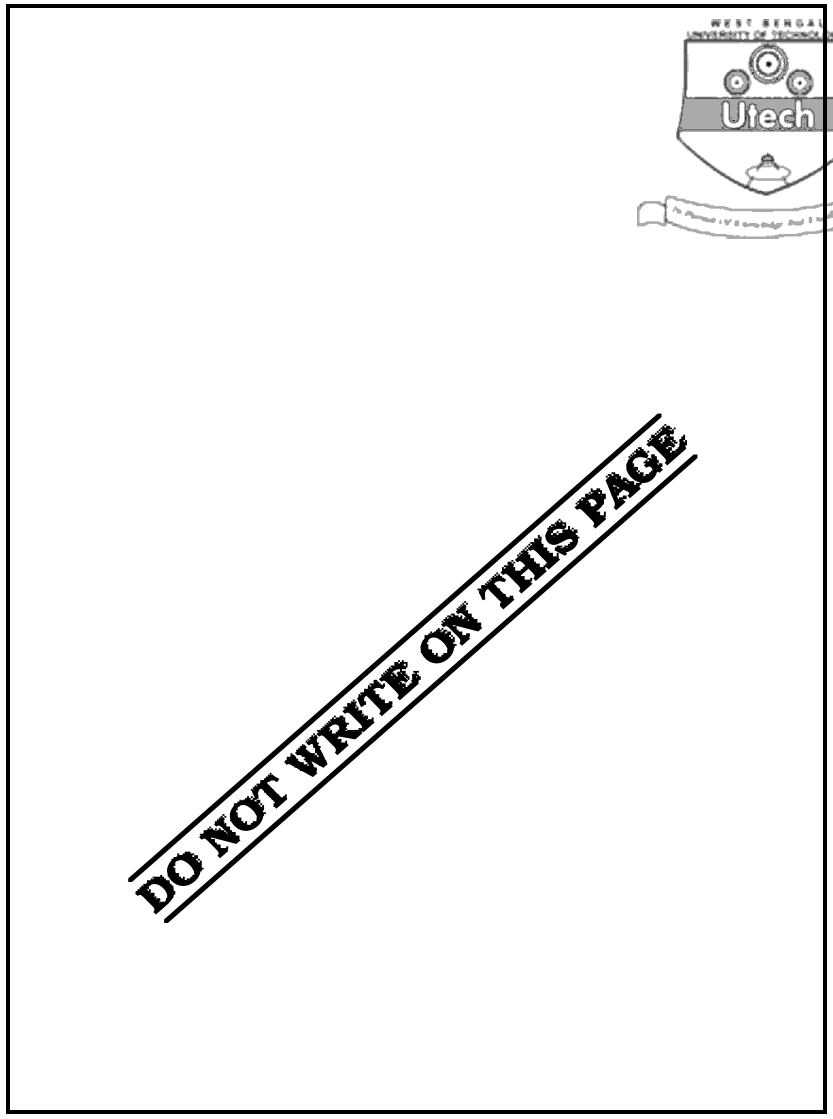
FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

Question Number											***Total Marks***	***Examiner's Signature***
Marks Obtained												

.....

Head-Examiner/Co-Ordinator/Scrutineer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CS/M.Tech(VLSI & MCS)/SEM-2/MVM-201/09
ARCHITECTURAL DESIGN OF VLSI SYSTEM
SEMESTER - 2

Time : 3 Hours] [Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer Question 1 and any *four* from the rest. 5 × 14 = 70

1. Answer any *seven* of the following : 7 ∞ 2

   a) What do you mean by a tristate logic device ?

   b) What do you mean by clock-skew ?

   c) What do you mean by floating gate devices ?

   d) What are the limitations of a cross bar switch ?

   e) What is a PAL ?

   f) What is an anti-fuse switch ?

   g) What do you mean by dynamic power dissipation of logic circuits ?

   h) State any two key features of VLIW architecture.

   i) What is a multi-computer architecture ?

2. a) Discuss in brief on the activities done in different phases of VLSI design flow.

   b) What do you mean by balanced tree based design of logic circuits ? What is a Glitch ? State any technique for its reduction. 8 + 6

3. a) Construct an optimized architectural design for the following algorithm :

```
prod : =1;
for ( i=1 to N )
        { prod:= prod * i;
        }
```

b) Discuss with a given example the use of Binary Decision Diagram for the storage and evaluation of a given Boolean Logic Expression.

c) State why NAND and NOR are preferred in CMOS based logic circuits in comparison to AND, OR logic. 6 + 5 + 3

4. a) Compare the features of RISC and CISC processor architecture. What do you mean by window registers and state how they are utilized in processes that are sharing data.

b) Discuss on the following operation in context to vector processors :

i) Vector load

ii) Vector store

iii) Scatter

iv) Gather. 6 + 8

5. a) Show that the efficiency of a pipelined processor is better than a non-pipelined one. What is non-linear pipeline ? State the critical factor related to these types of pipeline.

b) Draw the pipeline structure for the given time-stage diagram, also mention the whether there is any chance of collision for the given pipeline or not.

	1	2	3	4	5	6
S1	×					×
S2		≈		×		
S3			×			
S4				×	×	

7 + 7

6. a) State any one cache coherence protocol in context to multiprocessor architecture.

b) Discuss in brief on the major component of an FPGA chip. 4 + 10

7. Write short notes on : 7 + 7

a) Data Flow Architecture

b) UMA and NUMA architectures.

END