

Name :

Roll No. :

Invigilator's Signature :

CS/M.Tech(ECE-VLSI)/SEM-2/MVLSI-203/2011

2011

ANALOG INTEGRATED CIRCUIT DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

Answer any *three* of the following.

1. Explain clearly body-effect and channel-modulation in a MOSFET and incorporate them in a small signal MOS model.

14

2. What is meant by velocity saturation in an MOS device ? How does it affect the drain-source saturation voltage and the drain current ? Explain in detail deriving necessary expressions.

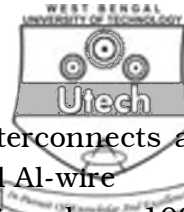
14

3. Draw neat circuit diagram of

- a) Inverting integrator and
- b) Non-inverting integrator

using switched capacitors for the input resistances and explain their working with particular reference to cancellation of parasitic capacitances.

14



4. Explain Elmore delay calculation for long interconnects and derive an expression for the delay. An isolated Al-wire 10 mm long and 0.4 micrometre wide is driven by a 100 X inverter. Estimate the total resistance and capacitance of the wire and the delay using Elmore Π -model. Choose wire capacitance as $0.1 \text{ fF}/\mu\text{m}$, also use sheet resistance, 27-milliohm/unit area. (The inverter on resistance for 1X is 15kohm, neglect inverter output capacitance) 7 + 7
5. Write short notes on any *two* of the following : $2 \times 7 = 14$
 - a) Relation between g_m and g_{mb} in a MOSFET.
 - b) Tow-Thomas biquad realization using switched capacitor
 - c) Critical electric field and its effect on $V_{D, \text{sat}}$
 - d) Subthreshold conduction.

GROUP – B

Answer any *two* of the following.

6. Explain with BJT circuit diagram the operation of differential amplifier in common mode and differential mode. Find out the expressions for common mode gain and differential mode gain. 7 + 7
7. Define current source and current sink. What are the drawbacks of practical current source/sink circuits ? Discuss how these problems can be overcome ? $5 + 2 + 7$
8. Write short notes on the following : (Answer any *two* from (a) to (e) and (f) $2 \times 4\frac{1}{2} + 5$
 - a) Band gap reference voltage
 - b) Wilson current mirror
 - c) Two stage Op-amp
 - d) CMOS two stage comparator
 - e) CMOS Voltage Controlled Oscillator
 - f) Active load/Mos resistor.

CS/M.Tech(ECE-VLSI)/SEM-2/MVLSI-203/2011

=====

