Name : ....

Roll No. : ....

Invigilator's Signature : ....

CS/M.TECH(ECE-VLSI)/SEM-2/MVLSI-203/2013

2013

ANALOG IC DESIGN

Time Allotted : 3 Hours   *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words

as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1.   Choose the correct alternatives for the following : $10 \times 1 = 10$

   i)   Equivalent resistance for parallel switch capacitor circuits

   a) T/C

   b) $4T/C$

   c) $2T/C$.

   ii)   Range and frequency to acquire lock is known as

   a)   lock in range

   b)   capture range

   c)   pull in range.

   iii)   Phase control Op-Amp is a type of

   a)   low noise Op-Amp

   b)   low power Op-Amp

   c)   high throughput Op-Amp.

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iv) Which of the following types of ADC gives the most high resolution output ?

    a) Flash type ADC

    b) Integrated ADC

    c) SAR.

v) How many MOSFETs are present in a minimized Op-Amp ?

    a) 6

    b) 8

    c) 12.

vi) Voltage gain of CD configuration is

    a) $\mu R_D / (r_d + R_D)$

    b) $- \mu R_D / (r_d + R_D)$

    c) $- \mu R_s$.

vii) In sample and hold circuit droop occurs due to

    a) internal storage capacitance

    b) internal diode

    c) both (a) and (b).

viii) Output resistance of MOS diode is

    a) g_m

    b) $1 / g_m$

    c) $-1 / g_m$.

ix) Equivalent resistance of bilinear switched capacitor circuits
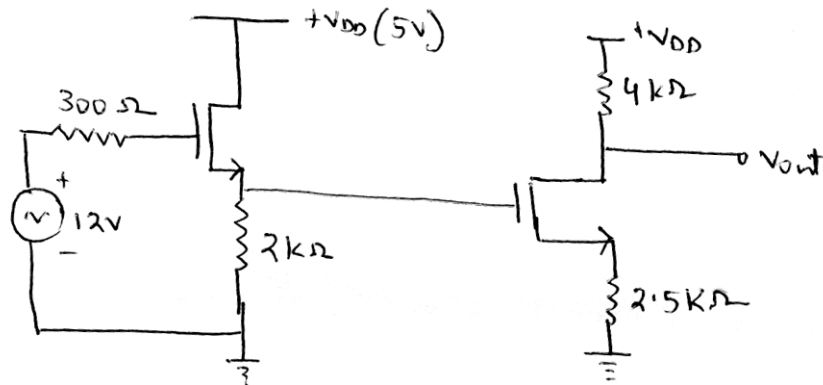
    a) $T/4$

    b) $4T/C$

    c) $(T_1 + T_2)/C$.

x) Peak to peak voltage difference between triangular and square output of a VCO is

    a) $0.5\ V_{CC}$

    b) $0.25\ V_{CC}$

    c) $0.35\ V_{CC}$.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following.   3 × 5 = 15

2. Calculate the overall gain of the circuit given below :

3. Calculate the total output resistance of a two-stage cascade current mirror circuit.

4. Describe how NMOS and PMOS can work as a diode.

5. Calculate the PSRR of an ideal Op-Amp.

6. Calculate the value of input combination, value of 1 LSB, percentage of accuracy and full scale voltage for 64 bit DAC. Assume reference voltage to be 12 V.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.   3 × 15 = 45

7. a) Calculate the equivalent resistance of a series parallel switched capacitor circuit.

    b) Determine the transfer function of a first order switched capacitor low pass filter.
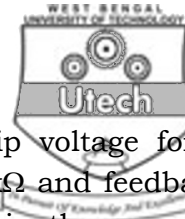
c) Calculate the positive and negative trip voltage for a comparator with input resistance of 5 kΩ and feedback resistance of 2 kΩ. Comparator works in the range of −12 V to + 12 V. Reference voltage for the circuit is 6 V.

4 + 5 + 6

8. a) Find expressions for lock in range and capture range of PLL.

b) Define maximum control voltage and V-F conversion factor of VCO. Deduce expression for them. 10 + (1 + 4)

9. a) Draw the small signal model for active load differential amplifier and calculate the total output resistance.

b) Calculate the CMRR of resistive load differential amplifier using half circuit analysis. 10 + 5

10. a) Calculate the output voltage of an 8 bit cycle DAC for which the digital input 11101110.

b) Calculate the DNL of 4 bit DAC with INL1 = 0·33 LSB, INL5 = − 0·94 LSB, INL7 = 0·5 LSB.

c) Describe the operation of an integrating DAC.

4 + 5 + 6

11. a) Draw the circuit diagram of a low noise Op-Amp and its noise model.

b) Calculate the small signal current gain and voltage gain of a common emitter amplifier with an emitter resistance. 8 + 7

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