	Utech
Name:	(4)
Roll No.:	A Grant of Exercising 2nd Excitors
Invigilator's Signature :	

CS/M.TECH(ECE-VLSI)/SEM-1/MVLSI-102/2011-12 2011

VLSI DEVICES AND MODELLING

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Group A is Compulsory and answer any four questions from Group B

GROUP - A

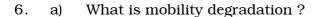
- 1. What is Punch-through?
- 2. What is channel-length modulation?
- 3. Mention the differences between EMOS and DMOS.
- 4. What are the limitations in increasing the power supply to reduce delay?
- 5. What is body effect?

2 + 2 + 3 + 3 + 4

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- b) How is the current effected due to vertical electric field in channel area of sub-micron devices? 4 + 10
- 7. a) What are the benefits of scaling?
 - b) How do you scale channel dimension, doping concentration, terminal voltages on the basis of constant field approximation? 4 + 10
- 8. a) What is drain induced barrier lowering?
 - b) Explain the action of double gate MOSFET with proper diagram. 7 + 7
- 9. a) Indicate the three regions of operations of a n-MOS transistor and explain them in detail.
 - b) How would they differ in case of p-MOS? 10 + 4
- 10. a) Illustrate the impact of Short-Channel effect on the threshold voltage.
 - b) Write the SPICE code for designing a NAND gate using CMOS. 4 + 10