

Name :

Roll No. :

Invigilator's Signature :

CS/M.Tech(VLSI)/SEM-1/PGMVD-105/2012-13

2012

DIGITAL VLSI CIRCUIT & SYSTEM

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

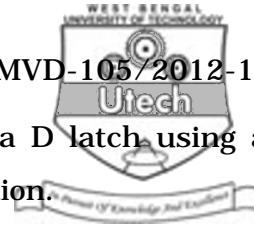
Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. 1 and any *four* from the rest.

1. Answer any *five* of the following : 5 × 2 = 10
- a) What is footed dynamic inverter ?
 - b) Sketch the transistor level schematic of a tristate buffer.
 - c) What are common formats of mask design. What is MOSIS ?
 - d) What is the problem when pMOS and nMOS are interchange their position in CMOS inverter.
 - e) What are the differences between the static and dynamic CMOS ?
 - f) Implement the CMOS flip-flop with two-phase non-overlapping clocks.



2. a) What are the four states of a CMOS logic gate and at condition they occur.
b) Why crowbarred level is unwanted ?
c) What is conduction complements ?
d) What do you mean by strength of a signal ? Explain why '0' is strong signal and '1' is week signal for nMOS.
e) What is transmission gate ? Why is it non-restoring circuit ? 2 + 2 + 2 + 5 + 4
3. a) What is CMOS Tristate inverter circuit. Why is it restoring logic gate ?
b) Implement a simple D flip-flop using a MUX.
c) Draw the restoring 2 : 1 MUX. Explain its opertion.
d) What do you mean by Functional Simulation. 3 + 3 + 4 + 5
4. a) What are the importance of Timing simulation and PPR (Planning, Placement and Routing) for VLSI Design.
b) What are the differences between the Full Custom and Semi-Custom design.
c) What is design specification. 10 + 3 + 2
5. a) Explain the Logical Effort and Parasitic Delay with example and also its importance.
b) What is Design Entry ?
c) What is the problem in dyanmic gate and how the problem will be overcome with domino logic. 5 + 5 + 5



6. a) Indicate the problems for designing a D latch using a CMOS transmission gate and its solution.
- b) Implement Synchronous and Asynchronous Resettable Latches and Flip-flops.
- c) Realize the following Boolean function using CMOS circuits.

.....
i) $Y = (D + E + A) (B + C)$
.....

.....
ii) $Y = AB + C (A + B)$
.....

iii) $Y = (AB + AB) C + D$
.....

iv) $Y = A (B + C) + DE$ 2 + 5 + 8

7. a) What are the advantages and drawbacks between ASICs and FPGAs ?
- b) Give the flexibility and performance analysis of ASIC, Microprocessor and FPGA.
- c) Implement the CMOS realization of the JK latch.
- d) Give the architecture of a FPGA. 4 + 4 + 3 + 4

