Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(ECE)VLSI/SEM-1/MVLSI-103/2010-11

2010-11

DIGITAL INTEGRATED CIRCUIT DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Short Answer Type Questions)

Answer *all* questions.

1. i) Find the dual of $Z = A + BC$.

   ii) Describe the working of a CMOS inverter with a neat diagram, explaining clearly how static current drawn from supply is zero.

   iii) Define the following for a logic circuit : P_w , t_p .

   iv) A digital computer has a common bus system for 16 register of 32-bits each. How many MUX are needed and what will be the size of each MUX ?

   v) What is Boolean expression language ?

   vi) *N*-mos is good in passing '0' and *P*-mos is good in passing a '1', justify. 2 + 3 + 2 + 2 + 2 + 3

GROUP – B

(Long Answer Type Questions)

Answer any *four* questions. 4 × 14 = 56

2. a) Briefly state the design principle of a static CMOS logic circuit.

   b) Using the above principle, design the following circuits (minimum transistor count is desired) :

   Carry and sum function in a binary adder with addend and augend inputs A and B and carry input C.

   4 + 4 + 6

3. Design a 2 : 1 MUX using transfer gates and using the same design a D-flip-flop (positive edge triggered). 4 + 10

4. Explain the working of a pseudo-NMOS logic circuit. What are it advantages and disadvantages ? A pseudo-NMOS inverter has the following parameters. $Kp' = 180\ \mu A/V^2$, $K_n = 540\ \mu A/V^2$, $V_{TN} = |V_{PT}| = 1V$. The W/L ratio are same for both. Estimate the value of V_{OL}. Device used has channel length > 1 μm. Justify the use of any equation and relation used. 6 + 8

5. Why we need CAD tools ? Briefly discuss about placement, floor planning and routing and why they need ? Draw the figure of PLA, where, $F1 = xy + x'z$; $F2 = y' + x'z$ and $F3 = xy + y'z$. 1 + 8 + 5

6. What are VLSI design cycle and physical design cycle ? Briefly describe about digital design process in CAD tools. 7 + 7

7. What do you mean HDL ? How many hardware modeling present in VHDL ? Brief discuss with proper example of various hardware modeling in VHDL. What do you mean by Top down design and Bottom up design style ? 1 + 1 + 8 + 4