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Name : .....

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Invigilator's Signature : .....

CS/M.Tech(ECE-VLSI)/SEM-1/MVLSI-103/2012-13

2012
DIGITAL IC DESIGN

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Objective Type Questions)

Answer the following questions : $7 \times 2 = 14$

1. a) For 0·18 um Technology, what is value of lamda ?

   b) What is Moore's Law ?

   c) What is another name of Channel less Gate Array ?

   d) What is key difference between PLA and PAL ?

   e) What is full form of VHDL ?

   f) What is key difference between Mealy Machine and Moore Machine ?

   g) What is Noise Margin for a logic family ?

GROUP – B

Answer any *four* of the following. 4 × 14 = 56

2. What is the difference between "Micron based Design Rule" and "Lambda Based Design Rule" ? Why EDA is required in VLSI Design ? What are differences between Full Custom Design and Std cell based Semi Custom Design ? Draw stick Diagram of 3 input NAND Gate. 2 + 3 + 4 + 5

3. Solve Euler Path Algorithm for the function $f = C\ (\ A + B\ )$! (! Means Bar). Draw Sick Diagram accordingly. Write short note on FPGA. What are various programming Techniques to program Programmable Logic Devices (PLD). 4 + 3 + 4 + 3

4. Draw *Y* chart for VLSI Design. Draw Flow of VLSI Design Cycle. Why HDL is required ? Draw Flow Diagram of Front End Design Flow. Write VHDL behavioural model for a D-Flip-Flop. 3 + 3 + 2 + 3 + 3

5. Draw flow diagram of High Level Synthesis. Draw flow diagram of Logic Synthesis. Draw BDD Diagram for function $f = abc + ab^{l}c + a^{l}bc^{l} + a^{l}b^{l}c^{l}$ using ordering of a ≤ b ≤ c. Create ROBDD Diagram and corresponding optimized Boolean expression. 3 + 3 + 4 + 4

6. Draw Flow Diagram of Physical Layout Automation. For Floor planning problem, what are inputs, outputs and Objective (Cost) function ? Write problem formulation of Global Routing using Steiner Tree. 4 + 5 + 5

7. What are key limitations of NMOS logic family ? Draw Voltage Transfer Characteristics (VTC) for CMOS inverter and show region of operation for PMOS and NMOS. If width of PMOS is increased how that can influence VTC Curve. Why CMOS Transmission gate is used instead of NMOS pass transistor logic ? Draw Transistor level circuit diagram of 2 input XOR function using CMOS logic and Pass Transistor Logic.

3 + 3 + 2 + 3 + 3