Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS / ME / M.TECH / SEM-2 / PGMVD-202 / 2011

2011

TESTING & VERIFICATION OF VLSI SYSTEMS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions taking at least *two* from each Group.

5 × 14 = 70

GROUP – A

1. a) What are the differences between testing and verification ? 2

   b) What are the different levels and types of testing ? 4

   c) Explain clearly with diagram the basic testing principle. 4

   d) What is functional testing ? 2

   e) What are 'VLSI chip Yield' and cost of a chip ? 2

2. a) What do you mean by 'Design for Test' ? What is 'Built In Self Test' ? 2 + 2

   b) Explain with the logic diagram the principle of operation of PRSG. 6

   c) What is BILBO ? Give the logic diagram of BILBO. 4

3. a) What is test Bench ? How are design verifications done for ASIC and FPGA ? 2 + 2

   b) Give the flow diagram for VLSI design. 4

   c) How can a sequential logic circuit be tested ? Discuss in detail with block diagram. 6

GROUP – B

4. a) What do you mean by stuck-at-1 & stuck-at-0 faults ? 2

   b) Assume that a logic circuit is to be implemented which is given by Boolean expression : $F = ab + cd$. The circuit employs only two input gates. Considering all single 'Stuck-at Faluts' on all check points, find out the number of check points and total fault sites. 8

   c) Assume that one of the pMOS transistors in a NAND gate has been stuck at 1 and one of the nMOS transistors in a NOR gate has been stuck at 0. Show what will be the outputs for all possible input combinations for both the gates. 4

5. a) What is fault simulator ? Give the block diagram of a fault simulator in a VLSI design process. 6

   b) What is 'ATPG' ? 2

   c) Write the different levels of Design verifications. 2

   d) How can a RAM be checked after manufacturing ? 4

6. a) What are the basic problem in testing the VLSI chip ? What do you mean by boundary scan ? 2 + 2

   b) Why is boundary scan technique used for testing the VLSI chips ? Give the block diagram of the architecture of JTAG and explain the operation. 2 + 6

   c) What is the need of ID register ? 2

7. a) Write the instruction set of JTAG and explain each of them. Show the flow chart for storing data into instruction register. 4 + 6

   b) What is the task of the TAP controller ? What is 'By Pass Register' ? 2 + 2

==========