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Name :	Olean
Roll No. :	A dearer (V/X markely part Confident
Invigilator's Signature :	

CS / ME / M.TECH / SEM-2 / PGMVD-202 / 2011 2011

TESTING & VERIFICATION OF VLSI SYSTEMS

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any five questions taking at least two from each Group.

 $5 \times 14 = 70$

GROUP – A									
1.	a)	What	are	the	differences	between	testing	and	
		verifica	tion ?)				2	
	b)	What a	re the	e diffe	rent levels an	d types of t	esting?	4	
	c)	Explain clearly with diagram the basic testing principle.							
								4	
	d)	What is	s func	ctional	l testing?			2	
	e)	What a	re VI	SI ch	ip Yield' and o	cost of a ch	ip?	2	
2.	a)	What d	What do you mean by 'Design for Test'? What is 'Built						
		In Self	Test'	?				2 + 2	
	b)	Explair	n with	the l	ogic diagram	the princip	ole of oper	ation	
		of PRS	G.					6	
	c)	What is	s BILI	30 5 0	Give the logic	diagram of	BILBO.	4	
304	72 (M	IE/M.TE	ECH)				[Turr	ı over	

3. What is test Bench? How are design verifications done a) for ASIC and FPGA? b) Give the flow diagram for VLSI design. 4 How can a sequential logic circuit be tested? Discuss in c) detail with block diagram. **GROUP - B** 4. a) What do you mean by stuck-at-1 & stuck-at-0 faults? 2 b) Assume that a logic circuit is to be implemented which is given by Boolean expression : F = ab + cd. The circuit employs only two input gates. Considering all single 'Stuck-at Faluts' on all check points, find out the number of check points and total fault sites. Assume that one of the pMOS transistors in a NAND c) gate has been stuck at 1 and one of the nMOS transistors in a NOR gate has been stuck at 0. Show what will be the outputs for all possible input combinations for both the gates. 5. a) What is fault simulator? Give the block diagram of a fault simulator in a VLSI design process. 6 b) What is 'ATPG'? 2

c)

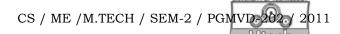
d)

Write the different levels of Design verifications.

How can a RAM be checked after manufacturing?

2

4



- 6. a) What are the basic problem in testing the VLSI chip? What do you mean by boundary scan? 2 + 2
 - b) Why is boundary scan technique used for testing the VLSI chips? Give the block diagram of the architecture of JTAG and explain the operation. 2+6
 - c) What is the need of ID register?
- 7. a) Write the instruction set of JTAG and explain each of them. Show the flow chart for storing data into instruction register. 4 + 6
 - b) What is the task of the TAP controller? What is 'By Pass Register'? 2 + 2

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