*Name* : .....

*Roll No.* : .....

*Invigilator's Signature* : .....

**CS/M.Tech/SEM-2/PGMVD-204-A/2012**

**2012**

# ADVANCED MICRO AND NANODEVICES

*Time Allotted* : 3 Hours *Full Marks* : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

Answer any *one* from ***Group-A***, any *two* from ***Group-B*** and any *two* from ***Group-C***.

## GROUP – A

Answer any *one* question : 1 × 14 = 14

1. i) An electron is confined to a infinite quantum well of length 2 nm. Find the two lowest enegy levels and corresponding wave functions. Draw the corresponding wave functions. 4

   ii) Find an expression for the Fermi energy in an intrinsic semi-conductor. 6

   iii) Using the following data find the band off set at the conduction and valance band edge at the GaAs and AlAs heterostructure junctions at room temperature. Draw the band line up and the fermi energy of GaAs, Al As and the heterostructure. 4

| Parameters | GaAs | AlAs |
|---|---|---|
| Electron effective mass | 0·066 m | 0·15 m |
| Hole effective mass | 0·051 m | 0·65 m |
| Energy gap | 1·42 | 3·0 |
| Electron affinity | 4·07 | 3·64 |

2. a) Derive an expression for the transmission probability of a particle across a barrier of heght '*V*' and width '*a*' for incident energy less than the barrier height. 7

b) What do you mean by resonant tunnelling ? 2

c) Explain the working of resonant tunnelling diode. Draw the current voltage relation and explain the occurrence of negative differential conductivity regimes. 5

## GROUP – B

Answer any *two* questions : 2 × 14 = 28

3. a) What are the factors on which the performance of a good CMOS depends ? 3

b) What is propagation delay ? On which parameters of the CMOS circuit does this propagation delay depend ? 2

c) What are the parasitic elements that are present in a CMOS circuit ? Discuss each with necessary diagram. 2 + 4

d) Discuss the merits and demerits of SOI technology. 3

4. a) What are the various effects that degrade the performance of nano-scale MOS devices ? Discuss the different methods that can be used to improve the performance. 3 + 3

b) How can Gate Engineering improve the performance of nano-scale devices ? Explain with special emphasis on the advantages of

i) Asymmetric Double Gate and

ii) FinFET. 2 + 3 + 3

5. a) What is a heterojunction ? How many types of heterojunctions are there ? 2 + 2

b) Explain with a suitable diagram the potential well formation in a lattice matched *n*-AlGaAs/undoped-GaAs heterojunction. 2 + 2

c) Compare the performance of a HEMT with that of a MOSFET. 3

d) What is the missing fourth passive circuit element ? Establish its existence logically. 1 + 2

## GROUP – C

Answer any *two* questions : 2 × 14 = 28

6. What is meant by epitaxy ? How is it different from melt growth process ? Which epitaxial technique is common for the growth of Si ? Name the basic steps involved in the growth of epitaxial layer of a silicon. How do you engineer band-gap in an alloy ? The "alloy $Al_xGa_{1-x}As$ over GaAs" is the most studied heterostructure. Explain. What is lattice misfit factor of an epitaxial film ? How does the critical layer thickness of an epitaxial film control the device properties ? What is called strained layer superlattices ?

1 + 1 + 1 + 1 + 2 + 2 + 2 + 2 + 2

7. MOCVD growth technique is preferred for the growth of III-V compounds. Why ? How is it different from conventional CVD ? Write the overall surface reaction for the growth of GaAs layer by CVD technique. Why is rigorous safety precaution necessary in MOCVD process ? The substrate in the reactor needs moderately high temperature for the growth by any CVD processes. Explain. Mention the important advantages and disadvantages of the four epitaxial growth techniques ( LPE, VPE, MOVPE and MBE ).

2 + 1 + 2 + 1 + 2 + 6

8. What is meant by C-V characterization of an MOS capacitor ? How do you measure MOS capacitance as a function of dc-bias ? Draw and mark the individual capacitance components of an ideal MOS capacitor showing the measurement at high and low frequency. What is referred as "deep-depletion" in C-V characterization curve ?

   An MOS device MD1 has an area of $1 \times 10^{-4}/cm^2$. What are its maximum and minimum capacitances ?

   ( Given : oxide thickness $t_{ox}$ = 1000 *A*, $\varepsilon_r$ = 3·9 for $SiO_2$ and $\varepsilon_r$ = 11·9 for Si and $\Phi_b$ = 0·35 eV.

1 + 2 + 3 + 2 + 2 + 4