Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (ME)/SEM-1/ME-105/2011-12

2011

SIGNAL CONDITIONING AND DATA ACQUISITION SYSTEM

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

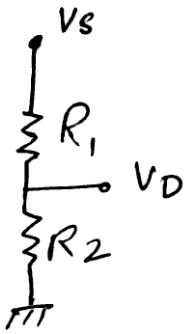
Answer any five questions. 5 × 14 = 70

1. a) Why impedance matching is important in signal conditioning ? Explain with an example.

b) Consider a sensor having I/O relationship as

$V_{out} = V_0 \exp(-\alpha . V_{in})$ where V_0 and α are constants. How can linear I/O relationship be obtained using proper signal conditioning ?

c) The divider circuit, as shown in figure given below has $R_1 = 5k\Omega$ and V_s = 5V. Suppose R_2 is a sensor whose resistance varies from 2 Ω to 4 kΩ as some variable varies over a range. Find (i) the minimum and maximum of V_D, (ii) the range of output impedance and (iii) the range of power dissipated by R_2.



4 + 3 + 7

2. a) What is 'lead compensation' ? Draw and explain a signal conditioning circuit that can be used to achieve lead compensation.

b) A bridge circuit is used with a sensor located 100 m away. The bridge is not lead compensated and the cable to the sensor has a resistance of 0.45 Ω/m. The bridge nulls with R_1= 3400 Ω, R_2 = 3445 Ω and R_3=1560 Ω . What is sensor resistance ?

c) Draw and explain the 'span' and 'zero' adjustment network. 5 + 5 + 4

3. a) What is notch out frequency ? Write down its expression. Design a notch filter for 50 Hz power line frequency rejection.

b) A measurement signal has frequency of < 1kHz, but there is unwanted noise at 1 MHz. Design a low pass filter that attenuates the noise to 1%. What is the effect of measurement signal at its maximum of 1 kHz ?

c) Draw and explain a voltage to current converter circuit with grounded load. 5 + 5 + 4

4. a) Draw and explain the circuit of an 'Instrumentation Amplifier'. Mention its advantages.

b) A sensor outputs a voltage ranging from – 2.4 to – 1.1 V. For interface to an analog to digital converter this needs to be 0 – 2.5 V. Design the signal conditioning circuit using 'Instrumentation Amplifier'.

c) What is 'ladder diagram' in relation with PLC ? Draw a ladder diagram for a motor having the following conditions.

The motor starts when the *NO* 'start' push button is pressed. A green light will glow at that time. The motor will run till *NC* 'stop' push button is pressed. When the 'stop' push button is pressed, the motor will stop and a red light will glow. 4 + 5 + 5

5. a) What type of ADCs are used for DAS and why ?

b) Draw and explain a Multichannel DAS with parallel conversion scheme. Mention its advantages.

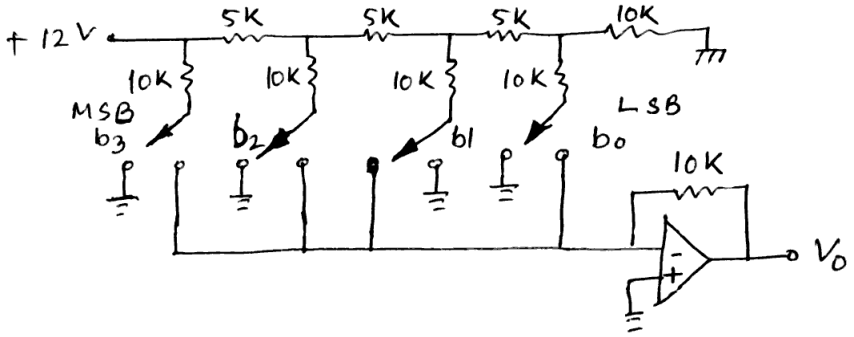
c) Why sample and hold circuit is necessary with *ADC* ? Draw and explain the operation of switched *OP-AMP* based sample and hold circuit. Mention its advantages.

2 + 5 + 7

6. a) Draw a *R*–2*R* ladder circuit of *n* bit *DAC* and prove that analog output voltage is equal to

$$V_o = -\frac{V_{ref}}{2^N}\cdot\frac{R_f}{3R}\left(2^{n-1}b_{n-1}+2^{n-2}b_{n-2}+\ldots+2^1 b_1+2^o b_o\right)$$

b) Determine the output voltage of the circuit as shown in the figure, when digital inputs are 1001 and 1101.



c) What is the percentage resolution of 4 bit *DAC* ?

8 + 4 + 2

7. a) Write the difference between MUX and DEMUX with examples.

b) Design 16 : 1 multiplexer using

(i) 2 : 1 MUX,

(ii) 4 : 1 MUX and

(iii) 8 : 1 MUX.

c) Implement the Boolean function

$F(A, B, C, D) = \sum(0,1,4,5,9,10,14,15)$ using multiplexer.

4 + 6 + 4

8. Write short notes on any *two* of the following : 7 + 7

a) Dual slope Integration ADC

b) Successive approximation ADC

c) Characteristics of DAC

d) Data logger.