



Name :

Roll No. :

Invigilator's Signature :

CS/M.Tech(ECE-COMM)/SEM-2/MCE-204C/2012

2012

INTEGRATABLE CIRCUITS & DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

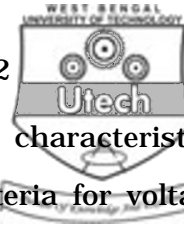
Answer question no. 1 and any *four* from the rest.

1. Answer the following questions in a brief : $7 \times 2 = 14$

- i) What are four generations of integration circuits ? Give the advantages of IC ?
- ii) What is enhancement mode transistor ? When the channel is said to be pinched - off ?
- iii) Why NMOS technology is preferred more than PMOS technology ? What are the different operating regions for an MOS transistor ?
- iv) Define threshold voltage in CMOS ? What is body effect ?
- v) What is channel-length modulation ?
- vi) What is Latch-up ?
- vii) Explain the principle of BICMOS inverter.

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[Turn over



- 2 a) Explain CMOS inverter voltage transfer characteristics with a neat diagram. What are the criteria for voltage threshold for high level and low level in inverter characteristics ?
- b) What is latch-up condition in CMOS circuits ? How it can be eliminated ? 5 + 2 + 5 + 2
3. a) What is current mirror circuit ? Draw the current mirror circuit and explain its operation.
- b) What is phase locked loop ? Mention two applications of PLL. 2 + 7 + 3 + 2
4. a) Design SR Flip-flop using CMOS technology and explain its operation.
- b) What is domino logic ? What are the advantages of domino logic over dynamic logic ? Discuss the charge sharing problems associated with domino logic circuit. 6 + 2 + 3 + 3
5. a) What is Transmission Gate (TG) ? Explain its operation.
- b) Design using TG :
- i) 2 : 1 multiplexer
- ii) D-flip flop. 2 + 2 + 5 + 5



6. a) Design the static logic circuit to implement the Boolean function $F = AB + AB'C + A'C'$. 6 + 5 + 3
- b) Design CMOS half adder circuit & explain the operation.
- c) Why NMOS is preferred for Pull Down and PMOS is preferred for Pull Up network.
7. Write short notes on any two of the following : 2 × 7
- a) Phase locked loop
- b) Delay of CMOS circuits
- c) Barrel shifters
- d) Switched capacitor amplifiers.

