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Invigilator's Signature : ....

CS/M. Tech (MC-VLSI)/SEM-1/PGMVD-104/2011-12

2011

MICROELECTRONICS TECHNOLOGY

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Objective Type Questions)

Justify any *ten* of the following questions.

10 × 2 = 20

1. a) 'Al' has been the preferred material for contact metallization.

   b) Si O_2 cannot be used as a diffusion mask for the dopant Ga.

   c) Sheet resistance is expressed in ohm/............. .
   (Fill in the blank)

   d) Oxide grows slower on <100> Si wafer than on <111> Si wafer.

   e) A mixture of KOH in water and isopropyl alcohol creates 'V-shaped' grooms in silicon.

   f) Reactive ion etching blends both of directionality and selectivity.

g) Si is the material of choice for CMOS VLSI technology.

h) Thermal evaporation has been replaced by sputtering in most of the silicon technologies.

i) Dry etching is preferred for small feature size.

j) Hydrofluroic acid is usually buffered with NH_4F to remove SiO_2.

k) Field oxide may be grown by wet oxidation.

l) TaN is used as a barrier material for making contacts from source/drain/gate to interconnect.

m) During thermal oxidation dopant redistribute themselves at the Si/SiO_2 interface.

n) The addition of Hcl during thermal oxidation stabilizes threshold voltage (V_{th}) of MOS.

GROUP – B

(Short Answer Type Questions)

Answer any *four* of the following questions.

$4 \times 5 = 20$

2. What is understood by "class 100" clean room ? For 0·25μm geometry devices what should be the size of the killer defect ? Name the major sources of organic contaminants. How do you remove the contaminants by a single cleaning step.

1 + 1 + 1 + 2

3. What do you mean by the word, 'thermal oxidation' ? Compare dry and wet oxidation techniqes. 2 + 3

4. Why is Local oxidation required in CMOS VLSI technology ? Give reasons for using pad oxide in case of LOCOS. Comment on the main concern of LOCOS process.

   1 + 2 + 2

5. Write down the important properties of a good photoresist. Compare them in terms of image transfer to the wafer. 2 + 3

6. What is meant by CMP process ? What is the purpose of using CMP ? Which etchant is used to remove Al selectively over Si and SiO_2 ? 2 + 2 + 1

GROUP – C

(Long Answer Type Questions)

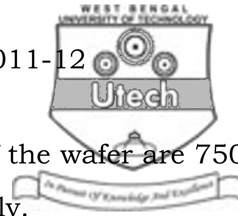
Answer any *two* of the following questions.

$2 \times 15 = 30$

7. What are the different usages of oxide layer in CMOS VLSI technology ? Which oxidation techniques are to be adopted for the fabrication of these oxide layers ? Starting with oxide growth kinetics develop the growth rate equation. Show that growth rate veries linearly for thin oxide whereas for thick oxide growth rate is parabolic. What factors affect oxidation process ? 2 + 2 + 5 + 2 + 2 + 2

8. What issues are to be considered in etching process ? Compare wet etching and dry etching.

   Calculate the Al average etch rate and etch rate uniformity on a 200 mm diametre silicon wafer, assuming the etch rates



at the centre, left, right, top and bottom of the wafer are 750, 812, 765, 743 and 798 nm/min respectively.

0·6μm of SiO_2 is to be etched; rate is 0·2μm/min. If etch selectivity of oxide relative to mask is 24 : 1 and to slightly over-etch you expose for 3·6 min, how thick should the mask be ?

Name different types of dry etch techniques. Which parameter is to be controlled to select the particular etching mode. 3 + 3 + 3 + 3 + 2 + 1

9. What kind of parasitic does arise from metal interconnects and metal contacts ? Discuss the problems of using Al as a metal in Integrated circuit with shallow junction ? How can these problems be minimised ?

   Why are silicides are promising material for VLSI circuits ? What is silicide technology ? Describe T_i silicide technology for CMOS process with suitable schematics.

   2 + 4 + 2 + 2 + 1 + 4