Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH(EIE)/SEM-1/EIEM-101/2011-12

2011

ADVANCED ELECTRONICS CIRCUITS

Time Allotted : 3 Hours *Full Marks* : 70

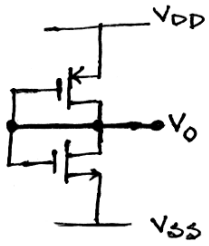
The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any ***five*** questions. 5 × 14 = 70

1. a) Using MOS (both *N*-channel & *P*-channel) draw the equivalent of active resistors. Find out the expression for current & channel conductance. Draw the small signal model. 3 + 4 + 2

   b) The MOSFETs (in the following figure) are used for voltage division. Find *W*/*L* ratio for both the MOSFETs that give V_0 of 1 V, if V_{DD} = + 5 V, V_{SS} = – 5V and *I* = 100 μA. Assume that V_{TN} = 0·75 V, V_{TP} = – 0·75 V, $K'_N = 2 \cdot 4 \times 10^{-5}\,\text{A/V}^2$, $K'_P = 0 \cdot 8 \times 10^{-5}\,\text{A/V}^2$. 5



2. a) Draw the ckt for differential amplifier using CMOS. Hence, find the value of A_{vds}. 3 + 6

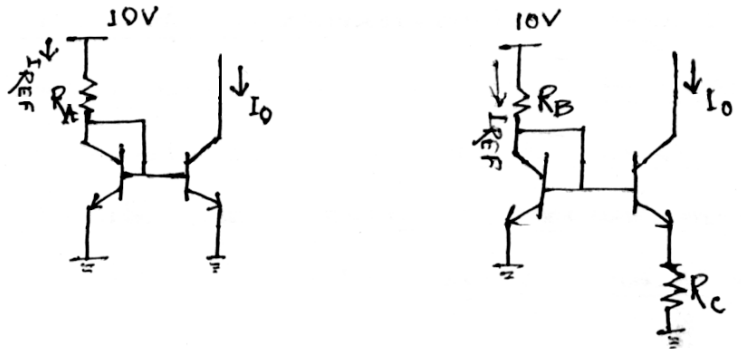
   b) Draw the small signal for two stage operational amplifier using BJT. 5

3. a) Why constant current source biasing is used in I.C. design ? Analyse the Widlar current source and obtain expressions for

      i) output current and

      ii) output resistance of this source. 2 + 6

   b)



The above two ckts are for generating a constant current I_0 = 10 μA which operate from a 10 V supply. Determine the value of all resistors. Assume V_T = 0·25 V. 6

4. a) Draw the basic structure of CMOS logic gate. Synthesize the Boolean function $F = \overline{A + B\,(C + D)}$ using CMOS. 2 + 7

   b) What is meant by transistor sizing and how is it done ? TWO MOSFETs having aspect ratio of $(W/L)_1$ and $(W/L)_2$ are connected in series. Determine the equivalent aspect ratio of this series combination. 3 + 2

5. a) Draw an 8-bit voltage scaling *D/A* converter and explain its operation with the *i/p-o/p* characteristic curve. 2 + 5 + 2

   b) Find the accuracy requirement for a resistor string consisting of *N* equal segments as a function of the number of bits *N*. If the relative resistor accuracy is 5%, what is the largest no. of bits that can be resolved to within ± 0·5 LSB ? 5

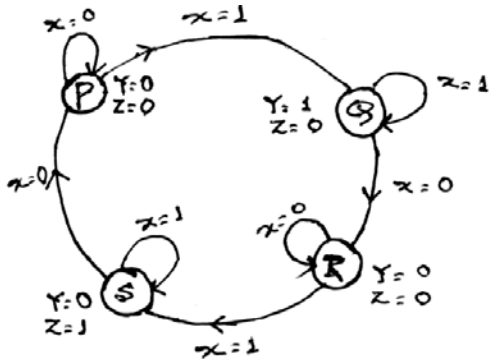
6. a) Explain with the help of circuit diagram the CMOS implementation of a clocked S.R. flip-flop. 9

   b) Using two-phase non-overlapping clock implement D-flip-flop. 5

7. a) Explain the importance of propagation delay and power dissipation in the logic circuit design. Draw the circuit diagram of a CMOS inverter and with reference to its voltage transfer characteristic obtain the matching condition. 3 + 2 + 5

   b) What are the advantages that result from matching ? 4

8. For the following state diagram design a clocked PLA FSM where x is the i/p and Y & Z are the o/p's.



9. Write short notes on any *two* of the following : 2 × 7

   a) IC fabrication process

   b) Bi CMOS inverter

   c) Charge distribution converter

   d) Current mirror.

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