*Name* : .....

*Roll No.* : .....

*Invigilator's Signature* : .....

**CS/M.Tech(EIE)/SEM-1/EIEM-101(A-3)/2009-10**

**2009**

# ADVANCED ELECTRONIC CIRCUITS

*Time Allotted* : 3 Hours | Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

Answer any *five* questions. 5 × 14 = 70

1. a) Obtain an expression for output current of a Wilson current source. What is the output resistance of the source ? 10

   b) For the Wilson current source as above the transistor parameters are $V_{BE}$ = cond = 0·7*V*, β = 50 and $V_A = \infty$. For $I_{REF}$ = 0·50 mA. Determine the current as shown in your diagram. 4

2. a) In what respect does a CMOS op. amplifier differ from a 741 bipolar op. amp. Internal circuit diagram of a CMOS op. amp. MC14573 is enclosed ( Fig.-1 ) for the following purposes :

      i) Explain the working principle of the various stages

      ii) Derive expressions for reference and input stage bias currents. 10

   b) Determine the IREF current in the above op. amp. if

   $\frac{1}{2}\ \mu_n e_{ox} = 20\ \mu A/V^2$ ; $\frac{1}{2}\ \mu_p e_{ox} = 10\ \mu A/V^2$

   $|\ V_{threshold}\ | = 0{\cdot}5V$ ; $V^+ = 5V$; $V^- = -5V$

   and $R_{set} = 225\ k\Omega$ 4

3. a) Enclosed ( Fig. 2 ) is the internal circuit diagram of a 741 op.amp. Identify the output stage of this op. amp. and make an analysis of the same for the following parameters :

   i) the output voltage limits

   ii) the output resistance. 11

   b) Explain the short circuit protection mechanism provided for the output stage. 3

4. a) Make an analysis of propagation delay in a CMOS inverter and obtain an expression for $t_{PHL}$ in terms of circuit parameters. 10

   b) Write an expression for $t_{PLH}$ by analogy to the $t_{PHL}$ and make at least three ( 3 ) useful observations for design. 4

5. a) Draw the basic structure of a dynamic MOS logic circuit and explain its operation using suitable waveform of the clock needed to operate the circuit Implement the logic $Y = \overline{A + BC}$ using the above circuit. 10

   b) What are the various sources of non-ideal effects of dynamic logic circuit ? Discuss any *one* of them. 4

6. a) What is an analog switch and what are its desirable characteristics ? 4

   b) Draw the circuit diagram of a CMOS transmission gate and explain its operation. Show the equivalent circuit for the operation when analog signal is positive. 10

7. a) Draw the circuit diagram of a CMOS implemented SR-flip-flop and explain its operation. 11

   b) State the assumptions based on which flip-flop switching is predicted. 3

8. a) What are the advantages of a BiCMOS inverter over a CMOS inverter ? Explain giving circuit diagram the basic concept of a BiCMOS inverter that incorporates bleeder resistors.

   b) Make an approximate estimate of the propagation delay of a BiCMOS inverter. 14

9. Write short notes on any *two* of following : 2 × 7

   a) Widlar current source

   b) Folded cascade CMOS circuit

   c) Sense amplifier

   d) Charge – redistribution converter.

Dia.

Fig.-1 MC14573 CMOS op-amp equivalent circuit

Dia.

Fig.-2