Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH (ECE)/SEM-3/MVLSI-302/2011-12

2011
ANALOG & DIGITAL VLSI CIRCUIT & SYSTEMS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Objective Type Questions)

1. Answer any *five* questions : 5 × 2 = 10

   a) The odd no. of inverter forms a close loop with positive feedback (ring oscillator), whose frequency of oscillation is ..... .

   b) If $K_n = 3K_p$, then what is the ratio of $(W/L)_p$ and $(W/L)_n$ to make $\beta_n = \beta_p$?

   c) For n input NAND gate driving a capacitance load C_L, what is the approximate expression of rising and falling propagation delay ?

   d) What is the minimum threshold voltage for which the leakage current through an off transistor ($V_{gs} = 0$) is 10^3 times less than that of a transistor that is barely on ($V_{gs} = V_{th}$) at room temperature if $n = 1.5$?

e) Consider a N-MOS transistor in a 180nm process with (W/L) = (4/2) lambda (0.36/0.18). In this process the gate oxide thickness is 40 angstrom and the mobility of electron is 180 cm^2/V sec at 78°C temperature. The threshold voltage is 0.4V. Plot *Id* vs V_{ds} graph for V_{gs} = 0, 0.3, 0.6, 0.9, 1.2, 1.5, 1.8V.

f) For a high-pass passive RC filter, derive it's gain and phase angle and plot it properly.

g) What is the caveats of Miller's theorem ? Explain it with examples.

GROUP – B

(Short Answer Type Questions)

Answer any *three* questions : $3 \times 5 = 15$

2. What are the reduction and concatenation operators in Verilog ? Explain with examples.
3. What are the different data types in Verilog ? Explain different net data types of wire.
4. What is logical effort ? Describe the relation between normalized delay(d), logical effort(f), electrical effort(h) and parasitic delay(p) d = f + hp.
5. What is back gate effect in MOSFET ? Express g_{mb} in terms of g_m.

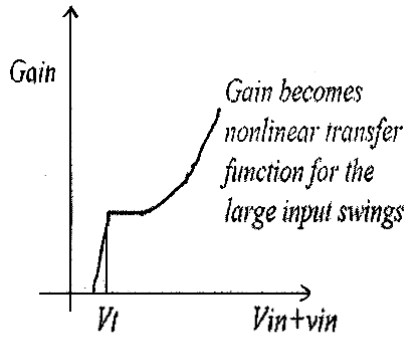
GROUP – C

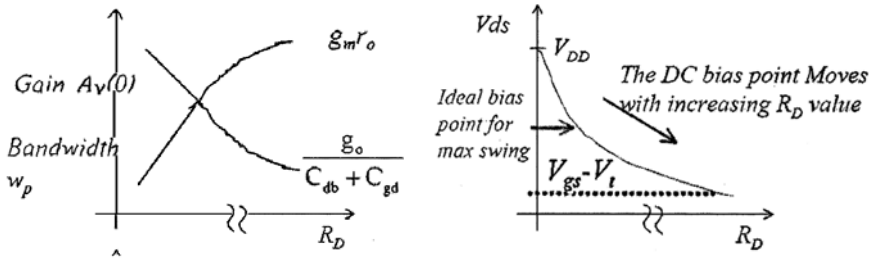
(Long Answer Type Questions)

Answer any *three* questions : $3 \times 15 = 45$

6. a) Write all the three equations of g_m and plot the graphs showing MOS trans-conductance as a function of overdrive voltage, drain current and W/L ratio.

b) Following three figures indicate the relation between DC gain $A_v(0)$, bandwidth and output swing as a function of R_d and input (both AC and DC) voltages for a resistive load NMOS inverter. From these figures give some important tradeoffs between DC gain $A_v(0)$, bandwidth and output swing and also make comments on improvement.





c) Design a 4 : 1 MUX using pass transistor logic with minimum no. of transistors. 4 + 6 + 5

7. a) Give the expression for calculating delay in CMOS circuit.

b) What happens to delay if you increase load capacitance ?

c) What happens to delay if a resistance is included at the output of a CMOS ?

d) Draw the logical circuit of a 4:1 MUX using tri-state buffer.

e) What are the limitations of pass transistors ?

f) Give the logical diagram of a tri-state buffer which eliminates the problems associated with the pass transistor.

g) Show with a diagram how a F/F that can be implemented using MUX. 2 + 2 + 2 + 3 + 2 + 2 + 2

8. a) What is Blocking and Non-Blocking Procedural Assignments in Verilog ? If you have to model a 4-bit right-shift register using Verilog then try to design the said example using blocking and non-blocking approach with always block.

b) Design a 4 : 1 MUX using component instantiation in Verilog where the basic building block in a tri-state buffer.

c) What is weak-sero-passing and strong-one-element ? Discuss with examples. 7 + 6 + 2

9. a) Sketch a 2 i/p NAND gate with transistor width chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the rising and falling propagation delay of a NAND gate driving *h* identical NOR gates using Elmore Delay including the resistance and capacitance in terms of R and C.

b) What is the logical effort of 2-input XOR gate ?

c) What is the use of delay statement in Verilog ? Is It synthesizable or not ? 9 + 2 + 4

10. a) Design a hex to seven segment decoder Verilog code using always block.

b) Write down the Verilog code of a 4-bit binary up counter and its test bench counterpart. 5 + 10