Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(ECE-VLSI)/SEM-2/MVLSI-201/2013

2013

PROCESSOR ARCHITECTURE FOR VLSI

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer question No. 1 and any *four* from the rest.

GROUP – A

1. Answer the following questions : 7 × 2 = 14

   a) If there is *n*-number of instructions and *k*-stage pipeline, then calculate the time required for a pipeline processing [consider as a time period of each clock pulse].

   b) What do you mean by array processor ? Give an example.

   c) What do you mean by scalar processor and vector processor ?

d) What are the fetch, decode and execution stages used by a TMS C6000 series DSP processor ?

e) What are main architectural advantages of a DSP processor over General Purpose Processor ?

f) Describe the role of a Co-processor as a processor accelerator with example.

g) What is the difference between ARM and Black finprocessor ?

GROUP – B

Answer any *four* questions from the following.

$4 \times 14 = 56$

2. a) Explain different types of Hardwired Controlled technique. 9

   b) Describe the steps of Microprogrammed Control. 5

3. a) Write the difference between RISC and CISC architecture. 4

   b) Write down the salient features of a SHARC Architecture. 4

   c) Let us consider a hypothetical architecture where there are 16 General Purspose Register (eg. R0, R1, R2, ... R15) and 4 operation codes/Instructions (e.g. Addition, Subtraction, Multiplication, Division). Then for the instruction

      MUL R3, R4

   what will be the horizontal and vertical micro instruction ? 6

4. a) Describe the different types of pipeline hazards and their solution. 10

   b) Describe Flynn's Architectural classification schemes of a computer system. 4

5. a) What are the architectural feature set of an ARM processor ? 4

   b) A C-language assignment is given like that $X = a + b$ how ARM processor solves this problem ? 5

   c) Solve (– 7) *3 using Booth's Multiplication Algorithm. 5

6 a) What are the advantages and disadvantages of multi-core processors ? 5

   b) Describe the generic architecture of multi-core processors. 4

   c) What are the salient features of coarse grained parallelism ? 5

7. a) Briefly explain the architecture of a processor implementing hyper-threading technology with the help of block diagram. 4

   b) Explain pictorially how a hyper-threading processor executes multiple thereads distributed over multiple applications. 5

   c) What are the salient features of fine grained parallelism ? 5

8. Explain two examples where a customizable data-plane can have performance benefits.