

# CS/M.TECH(ECE-VLSI)/SEM-2/MVLSI-201/2012 2012 <br> <br> PROCESSOR ARCHITECTURE FOR VLSI 

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Time Allotted : 3 Hours
Full Marks : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

## GROUP - A

( Objective Type Questions)

1. Answer any five of the following :
a) "Embedded systems are computers in disguise." Explain.
b) Discuss the general registers organization in ALU design.
c) Design a logic circuit taking a 4 : 1 MUX and some other gates to generate basic logical operations ( AND, OR, NOT and XOR ).
d) Design a circuit which is taking 4-bit input and increments its input by 1 .
e) Write a VHDL code which can convert a std_logic input into integer.

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f) What is the difference between vector and array processing?

g) What is the co-processor ?
h) How is the parallelism achieved using course grain architecture?

## GROUP - B <br> ( Short Answer Type Guestions) <br> Answer any three of the following. $3 \times 5=15$

2. Explain how Modified Harvard architecture is advantageous over Von Neumann architecture. What is Flynn's taxonomy ?
3. What are the essential components of an Embedded Computer ? Briefly describe the components of Embedded Computer.
4. You have two 4 -bit unsigned numbers. How you will get the product of the two numbers using combinational logic ? Describe with proper diagram.
5. What are the pipeline hazards ( data \& control ) ? Explain instruction pipeline having a jump instruction which will create hazards.
$2+3$
6. What are Moore and Mealy machines ? Design a 3-bit synchronous counter using FSM approach. $1+4$
7. Draw a simple ALU which takes two 8-bit numbers as inputs and after doing arithmetic/logic operation specified by the user, will store result in registers.

8. a) Discuss why CLA adder came into the picture in spite of having parallel ripple-carry adder. Then draw the block diagram of a 4-bit CLA adder briefly showing each part of it.
b) Write down a VHDL code of a 2's complement 4-bit ripple carry adder/subtractor. Discuss about its test bench file.

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3+5+5+2
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9. a) Suppose we have a data $i / p$ ( $n$ bit ). Now we have to scale this data $i / p$ by a factor 1.565876 . Design an architecture of a scale block which can accept this data and does scaling operation by cumulative addition till required scaling as per precision is achieved.
b) Design a 4 bit UP loadable Counter whose counting starts from 0100.
c) Design an arbitrary counter which can count the sequence $00,01,10,11,10,01,11$ in successive clock pulse with unique state representation. $6+4+5$
10. a) Using VHDL design a 2 : 1 MUX using only tri-state inverters.
b) How do you generate a Full Adder using only 2: 1 MUX in VHDL?
c) Draw and explain the serial binary 4-bit divider which will accept X [ 3: 0 ] \& Y [ 3: 0 ] as dividend and divisor and produce quotient Q [ $3: 0$ ] and remainder R [ 3: 0 ].
$3+4+8$

11. a) Implement a 4-input AND gate using CLB of FPGA where each CLB is a 4 -input Look-Up-Table ( LUT ) using both SRAM approach.
b) Implement the following two functions using Xilinx SRAM LUT based FPGAs :
i) $\quad \mathrm{X}=\mathrm{A}^{\prime} \mathrm{B}^{\prime}(\mathrm{C}+\mathrm{D})$
ii) $\mathrm{Y}=\mathrm{AK}+\mathrm{BK}+\mathrm{C}^{\prime} \mathrm{D}^{\prime} \mathrm{K}+\mathrm{AEJL}$
c) What is PSM ? Briefly discuss the different types of interconnects in FPGA. $5+5+5$
