



Name :

Roll No. :

Invigilator's Signature :

CS/M.Tech (ECE-MVLSI)/SEM-2/MVLSI-201/2012

2012

PROCESSOR ARCHITECTURE FOR VLSI

Time Allotted : 3 Hours

Full Marks : 70

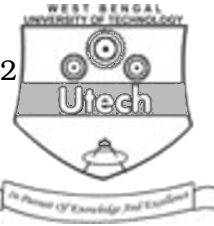
The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Short Answer Type Questions)

1. Answer the following questions : 7 × 2 = 14
- i) What is meant by course-grain parallelism ?
 - ii) What is flag register ?
 - iii) Distinguish between Von-Neumann and Harvard architectures.
 - iv) What are the operation of latch input and output enable of register ?
 - v) What do you mean VLIW ?
 - vi) State the differences between shared memory organization and distributed memory organization in MIMD.
 - vii) Compare RISC and CISC architectures of computers.



GROUP – B

(Long Answer Type Questions)

Answer any *four* of the following.

4 × 14 = 56

2. a) What is pipelining ?
b) Explain the concept with a suitable example.
c) What is speed-up of a pipelined architecture. 4 + 8 + 2
3. a) What do you mean by SOC (System On Chip) ?
b) Give brief description of three platform based SOC architecture. 4 + 10
4. a) What is the basic architectural and functional difference between Digital Signal Processor and General Purpose Processor ?
b) Why do we prefer Digital Signal Processor in signal processing field ?
c) With appropriate example, discuss about evolution of Digital Signal Processor. 6 + 4 + 4
5. a) Explain the UMA, NUMA & COMA architectural models for a multiprocessor system.
b) Describe briefly Flynn's taxonomy with appropriate diagrams. 7 + 7



6. a) Explain briefly RAW architecture with neat diagram.
- b) Describe with neat diagram of TMS320C6XXX series processor architecture. 6 + 8
7. a) Explain the status register and current program status register of ARM processor.
- b) What is exception ? Describe briefly the different types of exceptions handled in ARM processor.
- c) Explain the actions that ARM processor takes during an interrupt. 4 + 6 + 4

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