*Name* : .....

*Roll No.* : .....

*Invigilator's Signature* : .....

**CS/M.Tech (ECE-VLSI)/SEM-2/MVLSI-204D/2013**

# 2013
# PHYSICAL DESIGN AND TESTING

*Time Allotted* : 3 Hours *Full Marks* : 70

*The figures in the margin indicate full marks.*
*Candidates are required to give their answers in their own words as far as practicable.*

## GROUP – A
## ( Objective Type Questions )

Answer the following questions $7 \times 2 = 14$

1. Mention different fault models for testing combinational circuits on Si.
2. Mention different fault models for testing sequential circuits on Si.
3. What is input test pattern to detect Stuck-at-1 fault at the output of a 2 input NAND gate ?
4. What is minimum number of transistors needed to implement function Y = ABC + DE + F using CMOS logic.
5. State the differences between a control flow-based Control and Data Flow Graph (CDFG) and a data flow-based CDFG.
6. Compare black-box and white-box testing techniques.
7. Differentiate between a static hazard and a dynamic hazard.

**GROUP – B**

**( Long Answer Type Questions )**

Answer any *four* of the following. 4 × 14 = 56

8. Why Post Si Debug/testing is needed ? What is fault model ? Explain D-Algorithm using an example. Explain stuck ON and stuck OPEN Transistor Fault using 2 input NOR gate example. 3 + 2 + 5 + 4

9. What is key challenge for sequential circuit testing which does not exist in combinational circuit testing ? Draw circuit diagram of Scan Flip Flop and explain how it works. Draw block diagram of scan design/structure and explain its operation. 2 + 6 + 6

10. Draw circuit diagram of 2 input XOR gate using CMOS logic and CMOS transmission gate and compare number of transistors in both cases. Draw circuit diagram of D-Latch using CMOS digital gate and CMOS transmission gate and compare number of transistors in both cases. 7 + 7

11. What is clock skew ? What are sources of Clock Skew ? What is setup and hold time for a latch ? For a flip based sequential circuit, cycle time = 100ps, Setup time = 25 ps, Clock-skew = 10 ps, Combinational delay = 60 ps, Clock to Out Delay of Flop = 20 ps. Hold Time = 40 ps. What is setup margin and hold margin for the circuit ? 1 + 3 + 4 + 6

12. What does the pre-processing phase of High-Level Synthesis comprise of (State its necessity) ? What is functional verification and what are its objectives ? Write about the different techniques employed for functional verification of a design. 4 + 4 + 6

13. What are the different phases of verification in a typical VLSI design flow ? Differentiate between logic simulation and fault simulation. Illustrate the transport and inertial delay timing models with suitable examples considering nominal, rise/fall and maximum-minimum times of logic gates.

4 + 3 + 7