Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH(ECE)/SEM-2/MVLSI-205B/2013

2013

LOW POWER VLSI DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

1. Answer any *seven* of the following : $7 \times 2 = 14$

   i) Differentiate between single rail and dual rail logic.

   ii) What is electrical effort of a logic circuit ? What is its contribution in low power circuit design ?

   iii) What is fork circuit ?

   iv) What do you mean by 'speed versus area trade off' ?

   v) What is geometrical short channel effect (SCE) in MOS structure ?

   vi) What is narrow width effect (NWE) in MOS structure ?

   vii) What is clock gating ? Mention its role in low power design.

   viii) What is interconnect scaling in VLSI ? Mention its importance.

   ix) What do you mean by UDSA ? How does it differ from RSSA ?

GROUP – B

Answer any *four* of the following. $4 \times 14 = 56$

2. a) What are the various sources of power dissipation in a CMOS structure ? Explain with suitable diagrams.

   b) What do you mean by 'speed power trade off' ? Explain.

   10 + 4

3. With the help of neat diagram explain the impact of transistor sizing, gate oxide thickness and technology scaling in low power design. 5 + 5 + 4

4. a) With circuit examples, explain different transformation methods used for gate reorganization.

   b) Discuss the constraints on threshold voltage reduction in CMOS structure. 10 + 4

5. a) What do you mean by software level power estimation ?

   b) Discuss the advantage and disadvantage of SPICE power analysis method.

   c) Discuss how power estimation of a combinational circuit is carried out using entropy analysis.

   2 + 3 + 3 + 6

6. a) What are transition density and static probability ? Mention their role in power estimation.

   b) Compute total power of $Y = ab + c$ using transition density method. Given $P(a) = 0{\cdot}2$, $P(b) = 0{\cdot}3$, $P(c) = 0{\cdot}4$, $D(a) = 0{\cdot}1$, $D(b) = 2$, $D(c) = 3$.

   c) Draw the flow chart of Monte Carlo Simulation method.

   2 + 2 + 2 + 5 + 3

7. Write short notes on any *two* of the following : 2 × 7

   a) Adiabatic circuits.

   b) Relation of pipelining and parallelism with low power processor design.

   c) Role of power delay product (PDP) in low power VLSI design.

   d) Bus invert coding for low power I/O.

8. Discuss the role of the following techniques in low power design :

   a) Low swing signalling technique.

   b) Block disabling technique.

   c) Variable voltage technique.

   d) Data encoding technique. 3 + 3 + 4 + 4

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