



Name : .....

Roll No. : .....

Invigilator's Signature : .....

**CS/M.TECH(ECE-VLSI)/SEM-2/MVLSI-205B/2012**

**2012**

**LOW POWER VLSI DESIGN**

Time Allotted : 3 Hours

Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words  
as far as practicable.*

**GROUP - A**

**(Objective Type Questions)**

Answer the following.

7 × 2 = 14

1. If threshold voltage of transistor is increased. What happens to dynamic power and leakage power of digital gate ?
2. If channel length of transistor is increased, what happens to leakage power and delay of digital gate ?
3. What is the definition of Signal Probability ?
4. What is the definition of Activity Factor ?
5. For equal size (width) NMOS and PMOS device, which dissipates more leakage power when turned off ?



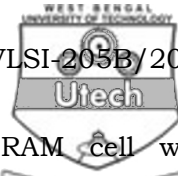
6. For a digital gate if load capacitance is  $C_L$ , what are the components of  $C_L$  ?
7. Under what input condition leakage power through a 3 input NOR gate is minimum ?

### GROUP – B

Answer any *four* questions from the following :

$$4 \times 14 = 56$$

8. Explain Dynamic power dissipation in VLSI circuit. What is Clock Gating and how can Clock gating reduce Dynamic Power ? How can VDD scaling reduce Dynamic Power ? Why is VDD scaling a problem in nano-device where VDD is already below 1V ?  
 $4 + 4 + 3 + 3$
9. Explain source of leakage power in VLSI circuit. What is stacking effect and how can it reduce significant leakage power ? Explain using 2 input NAND gate. What is sleep control ? explain using a diagram.  
 $4 + 6 + 4$
10. Explain critical path and non-critical path in VLSI circuits. What is set-up and hold requirement ? How power reduction is possible in non-timing critical path if the path is (i) device dominated and (ii) wire dominated ? Give an example of leakage power reduction in timing critical path.  
 $4 + 4 + 4 + 2$
11. Explain Short Circuit Power in VLSI Circuit. Explain Short Circuit Power Reduction techniques. Draw Power *vs* Delay Curve for a digital gate. Draw PDP (Power Delay Product) *vs* Size curve for a digital gate.  
 $4 + 4 + 3 + 3$



12. Draw circuit diagram of 6 Transistor SRAM cell with appropriate interface signals. What are the sources of leakage power in SRAM cell ? Why Dynamic Power in memory array is not as critical as data-path circuit ? How is Power reduction possible from 3 Transistor DRAM cell array to 1 Transistor DRAM cell array ? How power can be reduced in ROM array ?  $3 + 3 + 2 + 4 + 2$
13. How Feed forward inverter in Keeper Circuit can save power of a dynamic logic gate ? Under what condition Dynamic logic gates can provide less power with respect to Static CMOS gates ? Draw D-latch using (i) digital gates and (ii) pass transistor based CMOS circuit. Show how pass transistor based D-latch is more power efficient than digital gate based implementation.  $3 + 3 + 6 + 2$

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