



Name :

Roll No. :

Invigilator's Signature :

CS/M.TECH(ECE)/SEM-2/MCE-204C/2012

2012

INTEGRATABLE CIRCUITS & DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

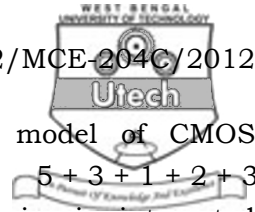
Answer Q. No. 1 and any *four* from the rest. $5 \times 14 = 70$

1. Answer the following questions : $7 \times 2 = 14$

- a) Draw the profile of electric field at $p-n$ junction for unbiased condition.
- b) What do you mean by scaling ?
- c) What are the advantages of differential amplifier ?
- d) What are the non-ideal characteristics parameters of differential amplifier ?
- e) Why very high value resistance cannot be realized using MOS transistor ?
- f) Define capture range and lock range related to PLL.
- g) What are the drawbacks of dynamic logic ?



2.
 - a) What do you mean by CPL Logic ?
 - b) Design a Full adder circuit using CPL Logic ?
 - c) Design a 4 : 1 Mux using TG Logic.
 - d) Describe the logic '0' and Logic '1' transfer of pass transistor Logic.
 - e) What is domino Logic ? 1 + 4 + 3 + 4 + 2
3.
 - a) What do you mean by DCVSL technique ? Justify your answer by a suitable example.
 - b) What do you mean by precharge evaluation Logic ? Describe with suitable Logic circuit.
 - c) Write a short note on NORA Logic.
 - d) Write the difference between latch and flip-flop. 5 + 3 + 4 + 2
4.
 - a) Design a four bit barrel shifter using mux and explain its operation.
 - b) Design a master-slave *D* flip-flop using TG Logic.
 - c) Write down the advantages and disadvantages of CPL and TG Logic. 6 + 4 + 4
5.
 - a) What are the advantages of switch capacitor circuit ?
 - b) Emulate equivalent resistance of series and shunt switch capacitor circuit.
 - c) How the effect of parasitic capacitance can be reduced in switch capacitor circuit.
 - d) Explain the operation of switch capacitor integrator circuit. 2 + 4 + 4 + 4
6.
 - a) Find the propagation delay time (τ_p) in CMOS inverter.
 - b) Explain the circuit operation of constant current mirror circuit using MOS transistor. How can the current mirror be used as an current amplifier ? What are the factors by which practical current mirror differs from ideal one ?



- c) Draw the small signal equivalent model of CMOS differential amplifier. 5 + 3 + 1 + 2 + 3
7. a) Describe about following types of noise in integrated circuit :
i) Thermal noise
ii) Flicker noise
iii) Burst noise.
b) Describe the noise model of bipolar junction transistor.
c) Explain the operation of one-three state output circuit. 6 + 4 + 4
8. a) With neat diagram explain variation of oxide related capacitance of NMOS with gate voltage.
b) Why input protection and off chip circuits are necessary in ICs ? With one circuit explain how ICs are protected from input side.
c) Draw and explain frequency response curve of BJT amplifier. 6 + 2 + 3 + 3

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