Name:	Utech
Roll No.:	A Agency (5' Exemple for 2ml Expellent)
Invigilator's Signature :	

CS/M.Tech (ECE)/SEM-2/MCE-204C/2013 2013

INTEGRATABLE CIRCUITS & DESIGN

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A (Multiple Choice Type Questions)

- 1. Choose the correct alternatives for any ten of the following : $10 \times 1 = 10$
 - i) Pseudo NMOS logic provides which of the following advantages?
 - a) Static power dissipation is less compared to CMOS logic
 - b) It is much faster compared to other logic
 - c) It requires less number of transistors compared to CMOS logic
 - d) It is more noise immune.

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- ii) NMOS is better than PMOS because
 - a) better noise immunity
 - b) faster
 - c) TTL compatible
 - d) better drive capability.
- iii) Metal used commonly in the metallization of CMOS circuit is
 - a) gold

b) silver

c) iron

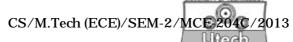
- d) aluminium.
- iv) CMOS logic gates are intrinsically
 - a) inverting
 - b) non-inverting
 - c) neither inverting nor non-inverting
 - d) none of these.
- v) How many transistors are required to realize the function F = AB + C(A + B) using CMOS logic ?
 - a) 10

b) 6

c) 8

d) 12.

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- vi) The disadvantage of domino logic is/are
 - a) only non-inverting structure can be realized
 - b) suffers from charge sharing
 - c) static inverter is required
 - d) all of these.
- vii) Typical value of sub-threshold slope is
 - a) 100 mV/decade
- b) 50 mV/decade
- c) 60 mV/decade
- d) 90 mV/decade.
- viii) The most important design point(s) about SOC is/are
 - a) time to market
 - b) power consumption
 - c) speed and performance
 - d) all of these.
- ix) BiCMOS means
 - a) two BJT circuits
 - b) two CMOS circuits
 - c) both BJT and CMOS circuits
 - d) none of these.

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- x) In VLSI test procedure(s) used is/are
 - a) diagnostic test
- b) functional test
- c) parameter test
- d) all of these
- xi) Design quality of a chip is measured on
 - a) testability
- b) reliability
- c) upgradability
- d) all of these
- xii) In circuit design procedure, parasitic components and their effect on transient performances are checked by
 - a) SPICE

b) LASI

c) VHDL

d) synthesis tool.

GROUP - B

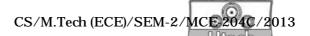
(Short Answer Type Questions)

Answer any three of the following.

 $3 \times 5 = 15$

- 2. Draw the fabrication steps of CMOS inverter (N-well process).
- 3. What do you mean by noise in an integratable circuit ? Discuss.
- 4. Draw the circuit of a CMOS full adder and explain its operation.

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- 5. Explain how a combination of switches and capacitors can be used to emulate a resistor.
- 6. Describe the following phenomena in MOS structre : $2\frac{1}{2} + 2\frac{1}{2}$
 - a) I-V characteristics
 - b) Channel length modulation.

GROUP - C (Long Answer Type Questions)

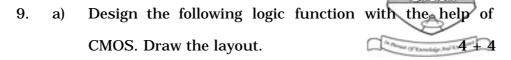
Answer any *three* of the following. $3 \times 15 = 45$

- 7. a) What do you mean by current sink and current source?
 - b) Explain the operation of a basic current mirror circuit. 6
 - c) What do you mean by differential pair?
- 8. a) Draw and explain the operation of MOS switched capacitor integrator and also find the expression for output voltage.6
 - b) What is phase locked loop? Explain its operation. Mention two uses of phase locked loop. 2 + 5 + 2

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$$Y = (A(D + E) + (BC))^{\top}$$

- b) Why do we use Pseudo NMOS?
- c) What is Domino CMOS logic? How can the cascading problem in dynamic logic be eliminated in Domino logic?
 5

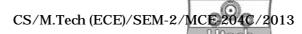
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- 10. a) What is the charge sharing problem in Dynamic CMOS logic? How can it be prevented?
 - b) What do you mean by CMOS transmission gate? 2
 - c) Design a XOR gate with the help of CMOS TG. 4
 - d) Design the following function with the help of CMOS TG:

$$F = AB + A^{\top}C^{\top} + AB^{\top}C$$

- 11. a) Design a CMOS clocked JK latch. Disucss the working principle of it. 4+4
 - b) Design a CMOS D-latch. Discuss the working principle of it. 3+4

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12. Write short notes on any three of the following:



- a) Multiplexer
- b) Decoder
- c) Barrel shifter
- d) CMOS NORA logic
- e) Digital adder.