

# CS/M. TECH (ECE-COMM)/SEM-2/MCE-204C/2012 2012 INTEGRABLE CIRCUITS \& DESIGN 

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

## GROUP - A

1. Answer any five from the following questions:
a) What are four generations of integrated circuits ?
b) Define the static resistance and the dynamic resistance of $p$ - $n$ diode.
c) Implement an XOR gate using CMOS transmission gate.
d) What is precharge-evaluate logic ?
e) What are the main constructional differences between an MOSFET and a BJT ?
f) What is the mass action law for the carrier concentrations in a semiconductor ? What is its significance?
g) What is the advantage of differential operation over single-ended signaling ?

## GROUP - B

Answer any five of the following questions. $5 \times 12=60$
2. a) What do you mean by channel length modulation ? How is drain current related with channel length modulation coefficient ? $2+2$
b) The reverse saturation current at 300 K of a p-n junction Ge diode is $5 \mu \mathrm{~A}$. Find the voltage to be applied across the junction to obtain a forward current of 50 mA . Given non-ideality factor $\eta=1$, Boltzmann's constant $k=1.38 \times 10^{-23} \mathrm{~J} / \mathrm{K}$, electron charge $q=1.6 \times 10^{-9} \mathrm{C}$.
c) Consider an $n$-channel MOSFET with $t_{0 x}=20 n m$, $\mu_{\mathrm{n}}=650 \mathrm{~cm}^{2} / \mathrm{V}-\mathrm{s}, \mathrm{V}_{\text {th }}=0.8 \mathrm{~V}$ and $\mathrm{W} / \mathrm{L}=10$. Find the drain current in the following cases :
i) $\quad \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{DS}}=1 \mathrm{~V}$
ii) $\quad \mathrm{V}_{\mathrm{GS}}=2 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{DS}}=1 \cdot 2 \mathrm{~V}$
3. a) Draw the circuit diagram of CMOS inverter and explain its operation using VTC curve.
b) Consider a resistive load inverter circuit with $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, K_{n^{\prime}}=20 \mu \mathrm{~A} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TO}}=0.8 \mathrm{~V}, \mathrm{RL}=200 \mathrm{k} \Omega$ and $\mathrm{W} / \mathrm{L}=2$. Calculate the critical voltages $\left(\mathrm{V}_{\mathrm{IL}}, \mathrm{V}_{\mathrm{OL}}\right.$, $\mathrm{V}_{\mathrm{IH}}, \mathrm{V}_{\mathrm{OH}}$ ) on the VTC and find the noise margins of the circuit.

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c) Derive the expression for inverter threshold voltage for CMOS inverter :
$V_{\text {th } I N V}=\frac{V \text { Ton }+\sqrt{\frac{k_{p}}{k_{n}}}\left(V_{D D}+V T_{O P}\right)}{\left(1+\sqrt{\frac{k_{p}}{k_{n}}}\right)}$
4. a) What do you mean by "Mosfet in weak inversion" ? Write down the drain current equation for MOSFET in weak inversion.
b) Design a 4:1 multiplexer circuit using TG switches. 4
c) Why dynamic logic can't be cascaded directly ? Implement the Boolean function $F=(\mathrm{ABC}+\mathrm{DE})^{\prime}$ using dynamic CMOS logic. $2+3$
5. a) A CMOS inverter has a power supply voltage $V_{D D}=5 \mathrm{~V}$. Using average current method calculate the fall time $i$ fall. $\mathrm{V}_{\text {out }}=\mathrm{V} 90 \%=4.5 \mathrm{~V}$ and $\mathrm{V}_{\text {out }}=\mathrm{V} 10 \%=5 \mathrm{~V}$. The output load capacitance is 1 pF . The nMOS transistor parameter is given as: $\mu \mathrm{nCox}=20 \mu \mathrm{~A} / \mathrm{V}^{2}$, (W/L) $n=10$, VT, $n=1.0 \mathrm{~V}$.
b) Design a static CMOS logic to implement the Boolean fuction $F=A B+A B^{\prime} C+A^{\prime} C^{\prime}$.
c) Draw the layout and schematic diagram of 2 -input static CMOS NOR gate and identity the corresponding components in the two drawings.
6. a) What are the problems associated with clock skem? 3
b) Design a NOR2 gate based CMOS SR Fatch and explain its operation. 4
c) Design a Full adder circuit using CMOS logic. 5
7. a) Draw the small signal equivalent circuit model of MOSFET and find output resistance. 3
b) With circuit diagram, explain the operation of MOS current mirror.
c) Derive the small signal voltage gain for common gate amplifier and compare it with common source stage amplifier. 5
8. Write short notes on any two of the following : $6+6$
a) Cascoding stage
b) CMOS differential amplifier
c) Domino Logic
d) Switched capacitor circuits.

