



Name :
Roll No. :
Invigilator's Signature :

CS/M.Tech (ECE)/SEM-1/MVLSI-102/2012-13

2012

VLSI DEVICE & MODELLING

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP - A

(Objective Type Questions)

1. Answer any *five* of the following : $5 \times 2 = 10$
- i) Draw the energy band diagram of a p-n-p transistor in the cut-off region.
 - ii) What do you mean by degenerate semiconductors ? Draw the energy band diagram of a degenerate p-n junction.
 - iii) What are the advantages of FET over BJT ?
 - iv) Write down the Shockley equation for JFET.
 - v) In which region is an FET operated for designing an amplifier ? Does it hold good for BJT also ?
 - vi) Why is polysilicon preferred as a gate material for MOSFET ?



GROUP – B

(Short Answer Type Questions)

Answer any *three* questions.

3 × 5 = 15

2. A p-n junction is made by doping a pure Si sample one side with P (doping concentration : 10^{16} cm^{-3}) and other side with B (doping concentration : 10^{17} cm^{-3}).

Given $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ for Si at room temperature.

- a) Which one is N_D and which one is N_A ?
 - b) Find V_{bi}
 - c) Draw the corresponding energy band diagram. 1 + 2 + 2
3. Briefly describe the effects of the fixed charges and the interface charges on the C-V characteristics of a MOS capacitor.
4. Draw the schematic diagram of an n -channel enhancement MOSFET and briefly describe its operation.
5. Explain what is meant by time dependent dielectric breakdown (TDDB).
6. A Si p-channel MOSFET is designed to have a saturation current of 8 mA when $V_{GS} = -5 \text{ V}$. Determine the ratio between channel width (Z) and channel length (L) by using the square law model. Given that the threshold voltage $V_t = -0.5 \text{ V}$, oxide thickness $t_{ox} = 40 \text{ nm}$ and channel mobility $\mu_p = 300 \text{ cm}^2 / \text{V.s}$.

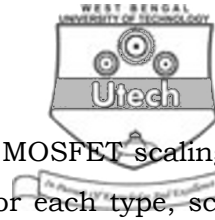


GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Plot the capacitance-voltage curve for an *n*-channel MOS capacitor and mark all the operating regions. Explain the nature of the curve for low and high frequencies.
- b) For an *n*-channel MOS capacitor find
 (i) C_i (ii) Q_d (iii) C_d (iv) C_{min}
 (Symbols have their usual significance) $(2 + 1 + 7) + 5$
8. a) Explain with a neat diagram the flat band voltage for a MOS system.
- b) For an Al-SiO₂-pSi MOS device at 300K, given that $N_A = 10^{16} \text{ cm}^{-3}$, $t_{ox} = 40 \text{ nm}$, $Q_{ec} = 5 \times 10^{10} \text{ cm}^{-2}$, $\Phi_m = 3.20 \text{ V}$, $\chi = 3.25 \text{ V}$, $E_g = 1.11 \text{ eV}$ at ϵ_r , (SiO₂) = 11.8.
 Calculate : (i) Φ_F
 (ii) Flat band voltage (Φ_{ms})
 (iii) Maximum depletion layer width (W_m)
 (iv) Threshold voltage (V_T) $5 + 10$
9. a) Draw the energy band diagram of a MOS capacitor for a *p*-type substrate for the following cases :
 (i) Accumulation (ii) Depletion (iii) Inversion
 (iv) Strong inversion.
- b) What do you mean by DIBL ? Explain with a neat diagram how this problem can be solved. $10 + 5$



10. State Moore's law. What do you mean by MOSFET scaling ?
How many types of scaling are there ? For each type, scale
the following parameters :

- i) $I_{D(\text{linear})}$ ii) $I_{D(\text{sat})}$ iii) Power iv) Power density
(v) C_{ox} 1 + 2 + 2 + (2 × 5)

11 Write short notes on any *three* : 3 × 5

- a) Metal semiconductor ohmic contact
 - b) Hot electron effects
 - c) Short channel effect
 - d) High frequency model of MOSFET.
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