Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH (ECE)/SEM-3/EC-906/2009-10

2009

VLSI DESIGN (ELECTIVE-V)

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions. 5 × 14 = 70

1. a) Implement the function $Y = \overline{A.B + C\,.\,(A + B)}$ with CMOS logic gates and verify the outputs for two possible combinations of inputs. 4

   b) Sketch a transistor level schematic for a CMOS 2 input-XOR gate and explain the truth table. 6

   c) Sketch a transistor level 2 : 1 restoring, inverting multiplexer using CMOS transistor. 4

2. a) Deduce the equations of currents of an ideal nMOS transistor. 8

   b) Discuss about the effects of non-ideal nMOS transistor in I-V characteristics. 4

   c) Define channel-length modulation. 2

3. a) Compare micron layout design rule with Lambda based design rule. 3

b) Sketch a stick diagram for a CMOS gate computing $Y = \overline{(A + B) . (C + D)}$ and estimate the cell width and height. 7

c) Sketch a 3 input NAND gate with transistor width chosen to achieve effective rise and fall resistance equal to that of a unit inverter and shows its gate and diffusion capacitances. 4

4. a) What are the different groups of digital function ? 2

b) What is meant by datapath operators ? 3

c) Draw a transistor level schematic for CMOS full adder. 5

d) Show how the number of required transistors can be reduced by using an alternative implementation. 4

5. a) What is the meaning of a continuum of accuracy in VHDL model ? 3

b) Write a VHDL code to describe the stucture of design. 3

c) Describe the VHDL code for circuit stimulus for four inputs. The periods of which are 80 ns, 40 ns, 20 ns and 10 ns respectively for the circuit schematically shown in the following figure and draw the simulation result. 5

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3

6. a) Describe how a VHDL file can be developed. 3

   b) Write a VHDL file for R-S flip-flop. 5

   c) Describe a NAND model in variable-delay mode. 4

   d) How can positive and negative logic be defined in VHDL code ? 2

7. a) What do you mean by Fixed-Delay model ? 2

   b) What are the differences between standard logic package and user defined package. 4

   c) What are the 46 values in 46-value unit delay model ? 2

   d) Write a VHDL code to define them. 3

   e) What are the technology rules ? 3

8. Write short notes on the following : 7 + 7

   a) Floorplanning

   b) FIFO.