Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH(ECE)/SEM-1/MVLSI-104/2010-11

2010-11

MICROELECTRONIC TECHNOLOGY & IC FABRICATION

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any five questions. 5 × 14 = 70

1. a) With the help of diagrams, describe how SiO_2 film is deposited in APCVD.

   b) Why is N_2 gas used in the above process ?

   c) Illustrate with plot the film deposition rate as function of substrate temperature and oxygen/hydride ratio.

   6 + 3 + 5

2. a) Explain with diagram the plasma generation mechanism used for PECVD.

   b) How does plasma improve the CVD process ?

   c) Why are HDPs (high-density plasmas) preferred ?

   7 + 4 + 3

3. a) Derive first and second Fick's diffusion laws.

   b) What are the differences between diffusions by interstitial and direct exchanging of atoms ?

   c) Plot the diffusion depth profiles for Boron and Phosphorous doping. 7 + 3 + 4

4. a) Describe the detailed process steps involved in patterning a wafer by photolithograph.

   b) Why are soft and hard baking necessary for lithography ? 9 + 5

5. a) Explain the choice of precursors used for GaAs film growth by MOCVD.

   b) Explain with diagram the setup for OM vapour generation mechanism. 6 + 8

6. a) Explain in detail the high-density ion generation mechanism used for ion implantation.

   b) Relate range of the implanted ions to ion energy.

   c) How are impurity concentration and depth of implantation controlled in an ion implantation process ?

   7 + 3 + 4

7. a) With diagrams, describe the steps in fabricating nMOS enhancement-mode transistors on a Si wafer.

   b) Why is sputtering preferred over evaporation technique for metallization ? 9 + 5