



Name :
Roll No. :
Invigilator's Signature :

CS/M. Tech (ECE-VLSI)/SEM-1/MVLSI-104/2011-12

2011

**MICRO-ELECTRONIC TECHNOLOGY AND
IC FABRICATION**

Time Allotted : 3 Hours

Full Marks : 70

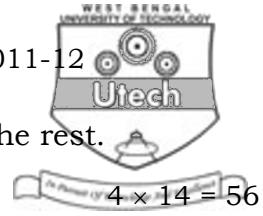
The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

Question No. 1 is compulsory and
answer any *four* from the rest

1. Answer the following questions : $7 \times 2 = 14$

- a) What material is used to create *n*-type doping ?
- b) What material is used to create *p*-type doping ?
- c) What material is used to create Gate of NMOS and PMOS transistor ?
- d) What material is used to create interconnect (or wire) ?
- e) What is the difference between Wafer and Die ?
- f) What is the name of technique to grow Silicon ingot ?
- g) What does CVD stand for ?



Answer any *four* questions from the rest.

2.
 - a) Describe Integrated Circuit Process flow chart.
 - b) Explain photolithography with example of $n +$ diffusion creation in p -substrate. 8 + 6
3.
 - a) Draw physical cross-section of CMOS inverter after fabrication.
 - b) Show all physical layers in the cross-section.
 - c) Identity Source, Drain, Gate and Channel Length of NMOS and PMOS in the cross-section.
 - d) Draw schematic diagram of the CMOS inverter with IN, OUT, VDD and GND nodes and show corresponding nodes in CMOS cross-section. 5 + 3 + 3 + 3
4.
 - a) Draw layout of CMOS inverter using Standard Cell Topology and show all the layers.
 - b) If channel length (L) is $0.5 \mu\text{m}$, PMOS Width (W_p) is $4.0 \mu\text{m}$ and NMOS Width (W_n) is $2.0 \mu\text{m}$, show those dimensions in layout picture.
 - c) Explain key features of standard cell layout design.
 - d) Why do Layout Design rules exist ? 5 + 3 + 4 + 2
5. Describe n -well CMOS fabrication steps with Mask definitions.



6. a) Explain Euler Path with the example of a CMOS gate which represents function $f = (A + B + CD) !$

- b) Draw Stick Diagram and layout of the same CMOS gate based on Euler Path solution. 7 + 7

7. Provide brief description on the following fabrication steps :

5 + 5 + 4

- a) Oxidation and CVD
- b) Diffusion and Ion Implantation
- c) Metallization.

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