Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(ECE-VLSI)/SEM-1/MVLSI-105B/2011-12

2011

EMBEDDED SYSTEMS FUNDAMENTALS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions taking at least *two* from each group.

GROUP – A

1. a) What is a watchdog timer ? Explain clearly. 4

   b) Explain the design of two systems, one in which a watchdog timer is based on a software design and another in which hardware circuit is used to realize the same. Explain the working of the circuit. 10

2. a) What is the role of cache memory (*cm*) in the design of an embedded system ? 4

   b) A 32 kByte of *cm* works in conjuction with a 16 MByte of main memory. Assume the line size to be 16 bytes and a 4-way set associative mapping, explain the different fields in the address bits and the size of each field. 10

3. a) Highlight the difference between normal and burst memory access. Illustrate with help of a timing diagram. 8

   b) How does a PCI bus work ? In this context explain the following terms :

      i) Bus arbitration

      ii) Bus parking

      iii) Little endian storage. 6

4. a) Why is interrupt important in an embedded system ? What is the difference between vectored and non-vectored interrupt ? 2 + 3

   b) What is interrupt latency ? Suggest some methods to reduce interrupt latency. Briefly discuss the interrupt mechanisms of 8051. 2 + 4 + 3

GROUP – B

5. a) Explain deadline in a real time system. What is the difference between hard and soft deadline ? 3 + 3

   b) What are periodic real time systems as against aperiodic real time systems ? What is the meaning of "hyperperiod" ? 3 + 3

   c) A system runs 3 periodic tasks having periods 5, 7 and 10 m seconds. What would be the hyperperiod ? 2

6. a) What do you understand by the term "Rate Monotonic Scheduling" (RMS) ? Explain why RMS is optimal in a restrictive sense. 3 + 3

b) Why is EDF scheduling classified as a dynamic scheduling method ? 3

c) What do you mean by "Real-time Operating System" (RTOS) ? What are the features of RTOS ? 2 + 3

7. a) What are the features of a RISC Processor ? 3

b) What do you mean by "Single Cycle Execution" ? 1

c) What is "Harvard Architecture" and what is the need of Harvard Architecture for RISC Processors ? 2

d) Why large number of registers are used in RISC Processors ? 1

e) Give the block diagram of AVR ATMEGA 64 and state the salient features. 4 + 3

8. a) Answer any *five* of the following : 5 × 1

i) What is the size of PC of 8051 ?

ii) What is the importance of ORG 0000 ?

iii) What is the use of PSW.3 and PSW. ?

iv) Why do we need subroutines ?

v) What are the differences between the following two instructions ?

MOVA, #46H

MOV A, 46H

vi) Which port of 8051 Microcontroller need pull-up resistor ?

vii) How many standard SFRs are present in 8051 Microcontroller ?

b) Answer any *two* of the following : 2 × 2

i) What is the difference between timer and counter ?

ii) What are the functions of XTAL1, XTAL2, ALE, RST ?

iii) Find the Machine Cycle for the following chips if XTAL frequency = 22 MHz

x) AT89C51 : 12 clocks per machine cycle.

y) DS89C4x0 : 1 clock per machine cycle.

c) Answer any *one* of the following : 1 × 5

i) Write down an assembly level language code for 8051 to display 9 on a seven segment LED, also show the interface.

ii) Calculate the time required for the below code :

```
Delay :  MOV R3, #250      ( Machine Cycle : 1 )
Here :   NOP               ( Machine Cycle : 1 )
         NOP               ( Machine Cycle : 1 )
         NOP               ( Machine Cycle : 1 )
         NOP               ( Machine Cycle : 1 )
         DJNZ R3, Here     ( Machine Cycle : 2 )
         RET               ( Machine Cycle : 2 )
```

Crystal Frequency = 11·0592 MHz, AT89C51 : 12 clocks per machine cycle.