



Name :

Roll No. :

Invigilator's Signature :

CS/M.Tech (ECE-OLD)/SEM-1/EC-903/2010-11

2010-11

DIGITAL INTEGRATED CIRCUITS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

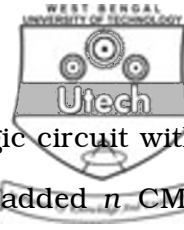
*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP - A

Answer Question No. 1 compulsorily and any *two* from the rest.

1. Write short notes on any *three* of the following : 3 × 5

- a) Switching power dissipation in digital CMOS circuits
- b) MTCMOS circuits
- c) Clock generator and distribution in an IC chip
- d) Adiabatic switching in CMOS circuits
- e) ESD protection in CMOS circuits
- f) Bi CMOS NOR2 circuit.



2. Explain clearly the working of a Bi CMOS logic circuit with a neat diagram. What is the function of the added n CMOS transistors ? Define h_{fe} for a BJT. 10
3. Explain current sinking and sourcing by a CMOS inverter. A high rate of change in output current in CMOS circuit causes problems. Explain how it can be avoided. A CMOS inverter operates from $V_{DD} = 5$ volts and has a capacitor load 100 pf. For a switching interval, $t_s = 5$ ns, estimate the $L di/dt$ drop in a bonding wire with $L = 5$ nh. Derive any expression used. 10
4. Define switching activity on a logic circuit. Discuss measures of reducing this parameter and give details of one architecture-level measure. 10

GROUP - B

Answer Question No. 5 compulsorily and any *two* from the rest.

5. Write short notes on any *one* of the following : 7
 - a) How are the operating points obtained from the voltage transfer characteristics of inverters for RS flip-flop ? Explain the significance of these points.
 - b) With the help of circuit diagram explain read operation of a DRAM. Why is the operation destructive ?



- c) Explain the working of a floating gate MOS and EEPROM.
6. a) Explain the working of a CMOS transmission gate. Point out how the ON resistance of the gate can be obtained. Sketch resistance versus output voltage plots for both the PMOS and NMOS transistors.
- b) With the help of circuit diagram explain the working of a XOR function implemented by CMOS transmission gates. 9 + 5
7. a) With the help of diagrams explain the precharge-evaluation cycle of a CMOS dynamic logic circuit. Mention the advantages of this over static logic circuit.
- b) Explain the working of a domino CMOS logic gates. 8 + 6
8. a) Explain with circuit diagram, the operation of a CMOS SRAM cell.
- b) Explain the read operation of a SRAM memory cell. Why are the bit lines maintained at a voltage $V_{DD}/2$ during read operation ? 6 + 8
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