



Name :

Roll No. :

Invigilator's Signature :

CS/M.Tech (ECE)/SEM-1/MVLSI-103/2012-13

2012

DIGITAL IC DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

$10 \times 1 = 10$

- i) Channel-less gate array is a sub-type of

- | | |
|---------|--------------------|
| a) FPGA | b) PLD |
| c) ASIC | d) Microprocessor. |

- ii) BDD is useful for

- | | |
|-------------------------|--------------------------|
| a) High level synthesis | b) Logic level synthesis |
| c) Testing | d) Timing analysis. |

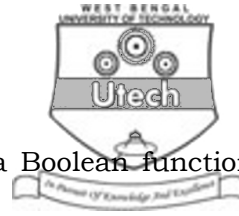
- iii) FPGA is a

- | | |
|-----------------------|-----------------------|
| a) Full custom design | b) Semi-custom design |
| c) Programmable ASIC | d) Structured ASIC. |

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- viii) What are the intermediate steps between circuit design and fabrication in VLSI ?
- a) Logic design
 - b) Physical design
 - c) Functional representation
 - d) System specification.
- ix) Dynamic logic circuit is
- a) Faster than static design
 - b) Slower than static design
 - c) Bigger than static design
 - d) None of these.
- x) VHDL is used for
- a) Timing analysis b) Layout diagram
 - c) Logic design d) RTL Coding.
- xi) Soft leakage problems of CMOS NORA structure can be reduced using
- a) TSPC logic
 - b) Zipper CMOS logic
 - c) NM logic
 - d) Cascaded domino logic.



xii) The sum of products expression of a Boolean function can be realized by

- a) AOI gates
- b) OAI gates
- c) Both (a) and (b)
- d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Write short notes on the following : $2 \times 2\frac{1}{2}$

- i) Standard cell design.
- ii) Routing.

3. Sketch a pseudo-nMOS gate that implements the function : 5

$$F = \overline{A(B + C + D) + E.F.G}$$

4. a) Draw the 2-input NAND gate using layout technique. 2

b) Sketch a 2-input DCVSL OR/NOR gate. 3



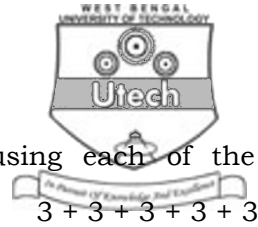
5. Explain the principles of Built-In Self-Test (BIST). What are the advantages and disadvantages of BIST ? 2 + 3
6. Explain the different kinds of physical faults that can occur on a CMOS chip and relate them to typical circuit failures. 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What kind of RAM cell would you use to control a configurable logic block in an FPGA ? Design the cell and outline the reasons for your choice. Explain the trade-offs between using a transmission gate or a tri-state buffer to implement an FPGA routing block. Design a static RAM memory cell using DCL logic. 1 + 5 + 4 + 5
8. a) Describe the *n*-well fabrication process with necessary diagram. 8
- b) Design a CMOS full adder using Domino logic gates. You may assume inputs and their complements are available. 7



9. Sketch 2-input XOR/XNOR functions using each of the following circuit techniques :

- i) Static CMOS
 - ii) Pseudo- n MOS
 - iii) Dynamic CMOS
 - iv) DCVSL
 - v) TG.
10. Consider the design of a CMOS compound OR-AND-INVERT (OA121) gate computing $F = \overline{(A + B) \cdot C}$
- a) Sketch a transistor-level schematic.
 - b) Sketch a stick diagram.
 - c) Estimate the area from the stick diagram.
 - d) Lay out your gate with a CAD tool using unit-sized transistor.
 - e) Compare the layout size to the estimated area. 5×3
11. a) Define “stuck-at-0”, “stuck-at-1” and bridging fault with example. $3 + 3 + 3$
- b) What are the goals of floor planning ? What are the constraints used in floor planning ? Difference between floor plan and placement. $1 + 2 + 3$



12. a) What are the advantages of dynamic logic over static logic ? Why dynamic logic cannot be cascaded directly ? How domino logic solve the cascading problem of dynamic logic ? Implement the logic function $f = (ab + ca)'$ using the smallest number of transistor using dynamic logic. $2 + 2 + 2 + 3$
- b) What is hardware description language ? What are the advantage and disadvantage of VHDL ? $2 + 4$
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