	Utech
Name:	
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Invigilator's Signature :	

CS/M.TECH(ECE-VLSI)/SEM-1/MVLSI-103/2011-12

2011

DIGITAL IC DESIGN

Time Allotted: 3 Hours Full Marks: 70

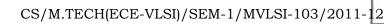
The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A (Short Answer Type Questions)

- 1. Answer *all* the following questions:
 - i) Distinguish between dual and complement of switching function. Find the dual and complement of F = A(B + C).
 - ii) Distinguish between ratioed and ratioless inverter.
 - iii) Define $V_{I\!L}$, $V_{I\!H}$, $V_{O\!L}$ and $V_{O\!H}$ of an inverter.
 - iv) N-MOS is good in passing a '0' and P-MOS is good in passing an 'l' justify.
 - v) Describe VHDL programming of full adder using behavioural modeling style. 2 + 3 + 2 + 3 + 4

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(Long Answer Type Questions

Answer any four of the following.

 $4 \times 14 = 56$

- 2. What do you mean HDL? How many hardware modeling present in VHDL? Briefly discuss with proper example of various hardware modeling in VHDL. What do you mean by Top down design and Bottom up design style? 1 + 1 + 8 + 4
- 3. What is meant by Domino Logic ? Design Domino Circuit with output F = A' + B'C.
- 4. Explain the principle of working of Transmission Gates.

 Realize the following function using Transmission Gate:

$$F = AB + BC + C'$$
 6 + 8

- 5. Why we need CAD tools ? Briefly discuss about Placement, Floor planning and Routing. Why they need ? Draw the figure of PLA, where, $F_1 = xy + x'z$; $F_2 = y' + x'z$ and $F_3 = xy + y'z$.
- Explain the advantages of CPL over Transmission Gates.
 Draw a neat diagram of a CPL based XOR gate and explain its working with particular reference to the level restoring PMOS gates.
- 7. What are VLSI design cycle and Physical design cycle?
 Briefly describe about digital design process in CAD tools.

7 + 7

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