Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(CSE)/SEM-2/PGCS-202/2012

2012

PARALLEL & DISTRIBUTED ARCHITECTURES

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions. 5 × 14 = 70

1. a) What is meant by Computer Architecture ? Mention some attributes of the Von-Neumann architecture.

   b) Categorize computer architectures according to Flynn classification rule. Draw clear diagram for each category and explain their properties. 7 + 7

2. a) What is the purpose of a clock in a computing system ? What are clock cycle and clock rate and what are their units ? If I_c be the number of instruction in a program and C be the average number of cycles per instruction and T is the processor cycle time, then compute the total CPU time needed to execute a program, assuming p = number of processor cycles for instruction decode, m = number of memory references and k as the ratio between memory cycle time and processor cycle time.

b) What is the importance of MIPS rate of a processor ? For the problem given above in question compute the MIPS rate and throughput also. 7 + 7

3. a) Consider a *k*-ary SIMD cube network. Answer the following questions :

i) How many nodes are there ?

ii) What is the network diameter ?

iii) What is the bisection bandwidth ?

iv) What is the node degree ?

b) Draw a 4-cube and label its nodes with addresses. What will be the next node of node number of 13 in dimension 0 ? How can you compute this automatically ? 8 + 6

4. a) What do you mean by spatial parallelism and temporal parallelism. Give suitable example of machines or architectures where you can observe such parallelism. Why do we say that spatio-temporal parallelism is found in a pipelined processor ?

b) Draw the space-time diagram of a 4-stage instruction pipeline to describe execution dynamics of 5 instructions through it. Compute the total execution time for the above and hence compute speedup, efficiency and throughput of the given pipeline. 7 + 7

5. Consider the following reservation table of a four stage pipeline with clock cycle T = 20 ns.

	1	2	3	4	5	6
S_1	×					×
S_2		×		×		
S_3			×			
S_4				×	×	

a) Derive forbidden latencies, initial collision vector and draw a state transition diagram.

b) Determine MAL and find out the pipeline throughput corresponding to MAL. Also determine the shortest greedy cycle. 7 + 7

6. a) What is a processor interconnection network and what is its requirement ? Write down advantages and disadvantages of single-stage and multi-stage interconnection networks.

b) Draw the multistage Omega network for 8 processors. Find out all possible routing functions for this network and write them in detail. 7 + 7

7. a) Write down parallel algorithms for adding elements of an array using SIMD CC and Mesh connected networks. Assume that the number of elements of that array matches exactly with the number of processors, for simplicity.

b) Trace the matrix multiplication processes in an SIMD CC system for the following two matrices. Use clear diagrams to show steps and data flow.

$$\begin{bmatrix} 2 & 3 \\ 2 & 1 \end{bmatrix} \text{ and } \begin{bmatrix} 5 & 4 \\ 1 & 2 \end{bmatrix}$$ 7 + 7

8. Write short notes on any *two* of the following : 7 + 7

a) Parallel speedup and efficiency

b) Crossbar network

c) Pipeline hazards

d) Vector processing.