CS/M.TECH (CSE)/SEM-2/CS-1003/09
PARALLEL AND DISTRIBUTED ARCHITECTURES (SEMESTER - 2)

1. ....
   Signature of Invigilator

2. ....   **Reg. No.**
   Signature of the Officer-in-Charge

Roll No. of the Candidate

CS/M.TECH (CSE)/SEM-2/CS-1003/09
ENGINEERING & MANAGEMENT EXAMINATIONS, JULY – 2009
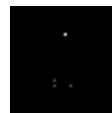## PARALLEL AND DISTRIBUTED ARCHITECTURES (SEMESTER - 2)

Time : 3 Hours]   [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. **This Booklet is a Question-cum-Answer Booklet.** The Booklet consists of **32 pages**. **First page** of the Booklet shows Instructions to the Candidates. The **questions** of this concerned subject commence from **Page No. 3**.
2. You have to answer the questions in the space provided marked 'Answer Sheet'. Write on both sides of the paper.
3. Fill in your Roll No. in the box provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. Use of Mobile Phone, Calculator or Log table is totally prohibited in the examination hall.
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, which will lead to disqualification.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

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FOR OFFICE USE / EVALUATION ONLY
Marks Obtained

Question Number										Total Marks	Examiner's Signature
Marks Obtained											

....
Head-Examiner/Co-Ordinator/Scrutineer

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PARALLEL AND DISTRIBUTED ARCHITECTURES
SEMESTER – 2

Time : 3 Hours]   [Full Marks : 70

*The figures in the margin indicate full marks.*

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions.   5 × 14 = 70

1. a) What are the potential problems of a static pipeline ? Name and explain them briefly.   3

    b) Describe the branch prediction scheme with a clear block diagram.   8

    c) How the pipeline performance can be improved by delayed branching ?   3

2. a) Draw a 3-cube architecture. Label the nodes with address bits. Write down the addressing schemes for routing between nodes.   6

    b) Write down the bitonic sort algorithm for cube-connected networks.   6

    c) Why is the above algorithm called 'bitonic' ?   2

3. a) What do you mean by physical and logical interconnections ? Draw 5 different types of physically connected networks.   5

    b) What do you mean by the following :   5

        i)   Functionality

        ii)   Network latency

        iii)   Bandwidth

        iv)   Hardware complexity

        v)   Scalability

        in relation to an interconnection network.
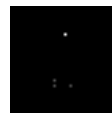
c)   What do you mean by node degree and network diameter of a network ? Evaluate them for a linear and a circular network having 8-processors.   4

4.   a)   Define the following performance measures for a parallel computing system :   4

        i)   Speedup

        ii)   Efficiency

        iii)   Throughput

        iv)   Degree of parallelism.

b)   What are the hardware and software bounds of parallel speedup ?   2

c)   Derive the relations between speedup and efficiency of a parallel system having n-processors.   8

5.   a)   What is average parallelism ? Derive an expression for the same.   4

b)   A parallel processor shows the following parallelism profile while executing a certain software.   4

Compute the average parallelism.

c)   Derive an expression for asymptotic speedup considering infinite number of available processors.   6
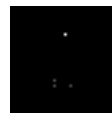
6.   a)   Describe the basic philosophy of a pipelined processor.   4

      b)   What are the differences between an instruction pipeline and an arithmetic pipeline ?   2

      c)   Derive the logic of a Carry-Save-Adder and design a 4-stage pipeline to multiply two 8-ply integers.   8

7.   a)   What is cache memory ? Why is it used in the memory hierarchy ? Draw a clear diagram to show its position in the memory hierarchy.   3

      b)   Define direct, associative and set associative mappings.   3

      c)   A computer uses 24-bit address bus and 32-bit data bus. If the cache memory size is 64 Kbytes and the main memory consists of 4M blocks of 4 bytes each, design and explain a direct mapping system, for the above example.   8

8.   Write short notes on any *two* of the following :   2 × 7

      a)   Crossbar interconnection network

      b)   Multi-stage switching network

      c)   Pipeline state transition.

END