Name :	
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Invigilator's Signature :	

CS/M.Tech (CSE)/SEM-2/MCSE-201/2012 2012 ADVANCED COMPUTER ARCHITECTURE

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

- 1. Answer any *seven* of the following : $7 \times 2 = 14$
 - i) Briefly state Flynn's classification.
 - ii) What are the conditions under which WAR and RAW hazards can occur ?
 - iii) How fault tolerance is achieved in interleaved memory organization ?
 - iv) What is the bottleneck of von-Neumann architecture ? How is it resolved ?
 - v) Find out the speed-up factor of pipelined architecture over non-pipelined architecture.
 - vi) Write down the routing functions for mesh connected Illiac network.

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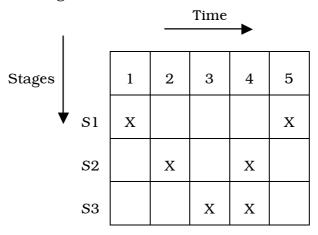


- vii) Briefly differentiate between superscalar and superpipelined architecture.
- viii) Compare the switching complexity of bus system, multistage network and crossbar switch.
- ix) State the bounds on MAL.
- x) Unifunction pipeline must be static whereas dynamic pipeline must be multifunction. Justify your answer.



Answer any *four* of the following. $4 \times 14 = 56$

2. Consider the 3-stage pipelined processor specified by the following reservation table :



- a) List the set of forbidden and permissible latencies and the collision vector.
- b) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.

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- c) List all the simple cycles & greedy cycles from the state diagram.
- d) What is MAL of the pipeline ?
- e) How to obtain an optimal MAL ? 1 + 1 + 3 + 2 + 7
- 3. a) Draw the configuration models of SIMD system.
 - b) Describe the characteristics of multistage interconnection network.
 - c) Write down the routing function for a hypercube network. 6+6+2
- 4. a) Draw the Clos network for N = 8 and derive Benes network from that.

b) Draw the multistage omega network for N = 8.

(5+4)+5

- 5. a) Describe Low-order interleaving using suitable block diagram.
 - b) Explain three different mechanisms to remove pipeline hazards.
 - c) Explain RAW, WAW, WAR. 5 + 6 + 3
- 6. a) Explain the execution of the vector instruction in a SIMD computer with 8 PEs :

$$A = (A_0, A_1, \dots, A_n - 1)$$

$$S (k) = \sum_{i=0}^{k} A_i \text{ for } k = 0, 1 \dots, n - 1$$

b) Describe the multistage hypercube network for N = 8. 9 + 5

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- 7. a) Describe the internal organization of element (PE) in SIMD system.
 - b) Write down the need of routing and masking functions in SIMD system.
 - c) Write down the characteristics of a switch box in multistage interconnection network.
 - d) How branching can be handled in pipeline ? $(\ 5+3+3+3\)$
- 8. Discuss about any *two* of the following topics : 2×7
 - a) $4^2 \times 3^2$ delta network
 - b) Parallel processing
 - c) RISC & overlapped register window
 - d) Arithmetic pipeline.