Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/ME/M.Tech./SEM-2/PGCSE-202/2011

2011

ADVANCED COMPUTER ARCHITECTURE

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. 1 of Section – A and any five Questions from Section – B & Section – C, taking at least two from each group.

SECTION – A

(Compulsory)

1. a) What do you mean by a scalable algorithm ? 2

   b) State Amdahl's Law. 2

   c) What are the advantages of the Harvard Architecture over the Von-Neumann architecture ? 2

   d) What is the advantage of configurable computing ? 2

   e) Why is pipelining called temporal parallelism ? What do you mean by spatial parallelism ? 1 + 1

SECTION – B

2. a) Compare the advantages and drawbacks between ASICs and FPGAs. 2

   b) With a block diagram explain the architecture of FPGA. 5

   c) With a diagram explain clearly how FPGA can be configured, Why FPGA can be used as a basic building block of "Re-Configurable Computing" ? 4 + 1

3. a) What do you mean by "Reconfigurable" Computing ? Give the block diagram of a "Re-Configurable Architecture" and explain the principle of operation. 2 + 5

   b) Give the block diagram of a 'Reconfigurable SIMD Architecture" and clearly explain the principle of operation. 5

4. a) What are the characteristics of a "Systolic Architecture" ? 2

   b) Give the block diagram of a Systolic Architecture to compute $y(n) = \sum x(n-k) \cdot h(k)$ for $k = 0$. Indicate the structure of the basic cell. Calculate the number of clocks required to deliver N number of outputs for such an Architecture. 4 + 1 + 1

   c) Give the block diagram of the Systolic architecture for matrix multiplications of two matrices of size (2×2). 4

5. a) What do you mean by overhead in "loop iteration" ? How can this be reduced to zero ? 2 + 2

   b) What is "circular addressing scheme" ? With an example clearly explain the need of such a scheme. 2

   c) Discuss a technique to design a barrel shifter for shifting an eight bit number to both directions (left/right). 4

   d) What do you mean by 'Single Cycle Execution" ? 2

SECTION – C

6. a) Prove that the total number of mesh points k or fewer jumps away from an arbitrary point in a $2D$ mesh is ($2k2 + 2k + 1$). (Ignore the case where the point is less than k jumps from the edge of the mesh.) 4

   b) Hence prove that a complete binary tree of height greater than 4 cannot be embedded in a $2D$ mesh without increasing the dilation beyond1. 4

   c) State and prove Brent's theorem. 4

7. a) Prove that :

   A *p-processor* PRIORITY PRAM can be simulated by a *p-processor* EREW PRAM with the time complexity increase by a factor of Θ (log (p)) (p is an integer). 4

   b) Show a dilation-1 embedding of an 8×2 mesh into a hypercube. Your diagram should clearly indicate which mesh position number gets mapped to which processor number on the hypercube. 4

   c) Write a CREW PRAM algorithm of your design that will automate the mapping in part (a). 4

8. a) What are the necessary and sufficient conditions for the existence of a dilation-1 embedding of a connected graph G to a hypercube with n nodes. 4

b) Given a node $(a_{k-1}, a_{k-2} \ldots a_1, a_0)_2$ in a shuffle-exchange network with 2^k nodes, which node will be exactly ($2k - 1$) traversals apart ? 4

c) Explain the importance of the following metrics for a network of processor nodes in parallel computer : 4

i) Diameter

ii) Bisection width

iii) Number of edges per node

iv) Maximum edge length.

9. a) Devise a CREW PRAM algorithm to multiply two $2^k \times 2^k$ matrices (k is an integer). 6

b) Find the time complexity of your algorithm. What will be the time complexity of the algorithm if the number of processors is p ? 6