Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (CSE)/SEM-1/PGCSE-103/2012-13

2012

PROCESSOR ARCHITECTURE & ORGANIZATION

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Short Answer Type Questions)

Answer any *five* of the following. 5 × 2 = 10

1. a) Write about Flynn's classification of computer.

   b) Explain the role of vector chaining and strip-mining ?

   c) What are the differences between CISC and RISC processor ?

   d) What are meant by forbidden latency and permissible latency ?

   e) Compare scalar and vector processing.

   f) RAR hazard can occurs in pipeline architecture ?

   g) What do you mean by linear and non linear pipeline ?

GROUP – B

(Long Answer Type Questions)

Answer any *four* of the following. 4 × 15 = 60

2. a) What is Memory interleaving ? Explain low order and high order memory interleaving ? 2 + 5

   b) Explain C-access, S-access and C-S access ? 3 + 3 + 2

3. a) Show that when N jobs are processed over a K-stage pipeline, the speed-up is

$$S = \frac{N \times K}{N + K - 1}$$ 5

   b) Consider the four stage pipelined processor specified by following reservation table :

	1	2	3	4
S1	X		X	
S2		X		
S3			X	
S4		X		X

   i) List the set of forbidden latencies and collision vector. 1 + 1

   ii) Draw the state transition diagram 3

   iii) List all simple cycles from state diagram 2

   iv) Identify the simple cycles among greedy cycles. 2

   v) Find out minimum average latency. 1

4. a) Explain 8 × 8 Omega network. Show the connection between 011 and 101. 4

   b) Explain $4^2 \times 3^2$ delta network. 4

   c) What do you mean by dataflow and control computer ? Draw the data flow graph to compute the expression : $\frac{a^2 + b^2}{a^2 - b^2}$. 2 + 2 + 3

5. a) What is control unit ? What is control word ? Considering a general purpose register based CPU organization with internal processor bus which is shared by the registers to transfer data, show the control signals needed to execute the following instruction ADD R1, R2, R3, where R1, R2, R3 are general purpose registers. 2 + 2 + 4

   b) What do you mean by micro-instruction and micro-routine ? What are the differences between horizontal format and vertical format of micro-instruction ? Write the format of micro-instruction. 2 + 3 + 2

6. a) What is virtual memory ? How is virtual memory implemented ? Considering 3 frames and the reference string 1, 0, 1, 1, 2, 3, 2, 0, 1, 2, 3, 2, 2, 1, find out the number of page faults using LRU page replacement algorithm. 1 + 3 + 4

   b) What do you mean by dynamic scheduling of instructions ? Write Tomasulo's algorithm of dynamic scheduling. What is VLIW processor ? 1 + 4 + 2

7. a) What is pipeline ? 1

   b) Find the speed up ratio for super pipeline, super-scalar architecture and superscalar-super pipeline. 9

   c) What is ILP ? What are the techniques for increasing ILP ? 2 + 3

8. a) What are

   i) T-gate ii) F-gate

   iii) T-F gate iv) Predicate and

   v) switch in data flow computer 10

   b) Explain odd-even transposition sorting algorithm. 5