Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(CSE)/SEM-1/MCS-101/2010-11

2010-11

COMPUTER ORGANISATION & ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* of the following. 5 × 14 = 70

1. a) State inclusion and coherence property of memory hierarchy.

   b) Prove that the effective memory access time of a memory hierarchy from M_1 to M_n is equal to
   $\left(h_1 t_1 + \left(1 - h_1 \right) h_2 t_2 + ... + \left(1 - h_{(n-1)} \right) t_n \right)$.
   Here h_1 = hit ratio of memory level M_i and t_i = memory access time of memory level M_i, where
   $i = 1, 2, 3, ... , n$.

   c) Consider the three-level memory hierarchy :

Memory level	***Access time***	***Capacity***	***Cost/unit***
Cache	T_1 = 25 ns	S_1 = 512 KB	C_1 = \$ 1·25
Main memory	T_2	S_2 = 32 MB	C_2 = \$ 0·2
Disk	T_1 = 4 ns	S_3	C_3 = \$ 0·0002

   Design goal is to achieve an effective memory access time T = 10·04 microsec with cache hit h_1 = 0·98 and main memory hit ratio h_1 = 0·9. Also total cost of the memory hierarchy is upper bounded by \$ 15,000. Calculate T_2 and S_3 of the system. 4 + 4 + 6

2. a) Perform following operations using 2's complement arithmetic :

   i) 17 – 5

   ii) – 30 – 21

   iii) – 25 + 11.

   b) Design a 4-bit carry look ahead adder using a diagram.

   c) Discuss hardwired and micro-programmed control unit of the processing unit. (3 ∞ 1) + 5 + 6

3. a) Perform $\frac{8}{3}$ using restoring division algorithm.

   b) State the different addressing modes of the instruction set architecture.

   c) State fetch-decode-execute cycle of a computing system.

   6 + 5 + 3

4. Write short notes on the following :

   a) Bus arbitration and control

   b) Flash memory

   c) Locality of reference

   d) Memory interleaving. 3 + 3 + 4 + 4

5. a) Identify different stages of a floating-point adder and design that floating-point adder pipeline. With a simple example of floating point addition, show the functionality of different stages in the designed floating-point adder. 3 + 3

   b) Design a pipeline multiplier with a CSA tree for multiplication of two six bit numbers. Modify the design of your six bit multiplier for multiplication of 32 bit numbers. Show the use of your modified pipeline multiplier for multiplication of two 32 bit numbers using a reservation table. 4 + 2 + 2

6. a) With respect to the performance of pipeline hardware unit, define the pipeline hazards. Categorize different types of pipeline hazard. 2 + 2

   b) With a simple example of two instructions *I* and *J* in a pipeline unit, describe three different situations of data hazards. Propose a method for detection of those three hazard situations. Present two suitable solutions to deal with possible data hazards. 3 + 2 + 2

   c) Discuss the use of Internal forwarding techniques with suitable example for improvement of performance in a pipeline system. 3

7. a) From definition of speed up, efficiency and throughput of a pipeline processor, deduce relationships between them. 2 + 2 + 2

   b) Suppose the time delay of the four stages of a pipeline are 65 ns, 95 ns, 50 ns and 90 ns respectively and the interface latch delay is 10 ns. Find out clock period, maximum frequency of this pipeline circuit and also find out speed up, throughput and efficiency of this pipeline circuit compare to the similar non-pipeline circuit. 4

   c) With simple example differentiate between the following :

      i) Unifunction and multifunction pipelines

      ii) Vector and scalar pipelines. 2 + 2

8. a) Present a situation of bottleneck in a pipeline system and also suggest two methods to overcome bottleneck situation. 2 + 2

b) How many number of 2 ∞ 2 switches and how many number of stages are required to design a 16 ∞ 16 omega network ? 2

c) Consider the five-stage pipelined processor specified by the following reservation table :

	1	2	3	4	5	6
S1	×					×
S2		×			×	
S3			×			
S4				×		
S5		×				×

i) What are the forbidden latencies and the initial collision vector ?

ii) Draw the state transition diagram for scheduling the pipeline.

iii) Determine all simple cycles, greed cycle and MAL.

2 + 3 + 3