Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M-TECH (CSE)/SEM-1/CST-613/2010-11

2010-11
ADVANCED COMPUTER ARCHITECTURE & OPERATING SYSTEMS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions taking at least two from each group.

GROUP - A

1. a) What do you mean by performance of a processor ? What are the different parameters used to measure the preformance of processors ? 3

   b) Compare RISC and CISC with examples. 3

   c) A program with the following instruction mix was run on a computer operating with a clock signal of 100 ns : 30% arithmetic instructions, 50% load-store instructions and 20% branch instructions. The instruction cycle time for these types are 1, 0·6 and 0·8 ns respectively. Calculate the CPI for this computer. 4

   d) What do you mean by parallel computers ? What are the different types of parallel computers ? Explain each of them in brief. 4

2. a) Design a 28-bit multiplier non-linear pipeline using CSA. Show its reservation table. 4

   b) What do you mean by the pipeline hazards ? What are the different types of pipeline hazards ? Explain each of them. 6

   c) Compare super-pipelining, super-scalar, VLIW processors. Give example for each. 4

3. a) Define vector processor. Why most vector processors have pipeline structures ? 2

   b) What are the strip mining and vector stride in respect of vector processors ? 4

   c) In an SIMD array processor of 8 *PE*s, the sum *S(k)* of the first k components in a vector A is desired for each k from 0 to 7. Let $A = (A_0, A_1, ..., A_7)$. We need to compute the following 8 summations :

   $$S(k) + \sum_{1=0}^{k} Ai \; ; \quad \text{for } k = 0, 1, ..., 7.$$

   Discuss how data-routing and masking are performed in the processor. 5

   d) Explain how an unauthorized access to a memory module can be prevented in multi-port networks. 3

4. a) What is meant by cache miss penalty ? Suggest one technique to reduce it. 3

   b) A digital computer has a memory unit of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words. How many bits are there in the tag, index, block and word fields of the address format ? 3

c) What is meant by cache coherence problem ? Discuss about Snoopy protocol for this problem. 3

d) What is/are objective(s) of data flow computers ? Compare it with control flow architecture with suitable diagram. 5

GROUP – B

5. a) Describe how interrupt technology helps out to implement multiprogramming system.

b) Explain the role of PCB for process management ? Explain relative advantages of 7-state models for process state transition with 5-state model.

c) Consider the following set of processes, with the length of the CPU burst time given in milliseconds and arrival time :

Process	Burst time	Arrival time
P1	4	1
P2	2	2
P3	4	3
P4	3	4
P5	2	5

Draw Gantt charts illustrating the execution of the process using pre-emptive SJF (or SRTF) and average waiting time. 3 + (3 + 5) + 3

6. a) Explain mutual exclusion for concurrent processes.

b) How are mutual exclusion, progress and bounded waiting preserved for counting semaphore ?

c) Why is thread required ? Explain different thread types. Compare User level thread and Kernel level thread.

2 + 5 + (2 + 2 + 3)

7. a) Consider a system with a total of 150 units of memory, allocated to the three processes as shown below :

Process	Max	Hold
P1	70	45
P2	60	40
P3	60	15

Apply the Banker's algorithm to determine whether it would be safe to grant each of the following requests. If yes, indicate a sequence of terminations that could be guaranteed possible. It no, show the reduction of the resulting allocation table.

Also explain the situation below.

i) A fourth process arrives, with a maximum memory need of 60 and initial need of 25 units.

ii) A fourth process arrives, with a maximum memory need of 60 and an initial need of 35 units.

b) Explain logical address. Describe paging and its advantage. (5 + 2 + 2) + (1 + 4)

8. a) What is demand paging ? Compare FIFO, LRU and Optimal page replacement algorithm with the following reference string 1, 0, 2, 2, 1, 7, 6, 7, 0, 1, 2, 0, 3, 0, 4, 0, 3. Compute the hit ratio. Assume that the available free frames are 3 and those are initially empty. Also give your comment on the effectiveness of each algorithm.

b) What is thrashing ? (2 + 9) + 3