*Name :* .....

*Roll No. :* .....

*Invigilator's Signature :* .....

**CS/M.Tech (CSE)/SEM-1/CST-912/2011-12**

**2011**

# ADVANCED ARCHITECTURE

*Time Allotted :* 3 Hours *Full Marks :* 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

## GROUP – A

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for the following : 10 × 1 = 10

   i) The utilization pattern of successive stages in the pipeline is specified by

      a) space-time diagram

      b) reservation table

      c) both (a) & (b)

      d) none of these.

   ii) If the memory chip size is 256 × 1 bits, then the number of chips required to move up 1 kilobyte of memory is

      a) 32 b) 24

      c) 12 d) 8.

iii) Forbidden latency means

a) distance between any two checkmarks in the same row of the reservation table

b) distance between any two checkmarks in the same column of reservation table

c) distance between all the checkmarks

d) none of these.

iv) In fourth generation computers, the main technology used is

a) Transistor

b) SSI

c) MSI

d) LSI and VLSI.

v) The minimum number of operands with any instruction is

a) 1 b) 0

c) 2 d) 3.

vi) Pentium-IV works on

a) control flow mechanism

b) data flow mechanism

c) demand driven mechanism

d) all of these.

vii) More RAM is required in

a) CISC b) RISC

c) Vectors d) None of these.

viii) CISC microprocessors have

a) Complex machine instruction

b) Best addressing capacity

c) Both (a) & (b)

d) None of these.

ix) Real pipelines are

a) Linear

b) Non-linear

c) Exponential

d) None of these.

x) It is possible to achieve parallelism

a) with and within the CPU

b) with many CPUs only

c) without CPUs

d) all of these.

## GROUP – B

### ( Short Answer Type Questions )

Answer any *three* of the following. 3 × 5 = 15

2. Prove that a *k*-stage linear pipeline can be at most *k*-times faster than that of a non-pipelined processor.

3. What is Von-Neumann concept & its bottleneck ?

4. What is reservation table ? What is the basic difference of it with space-time diagram ? 3 + 2

5. Compare RISC with CISC.

6. Explain arithmetic pipe line and instruction pipe line with suitable diagram.

## GROUP – C

### ( Long Answer Type Questions )

Answer any *three* of the following. 3 × 15 = 45

7. a) What is pipeline processor ?

   Define — speed up, efficiency, throughtput depending on pipeline processor.

   b) Write down the difference between parallel processing and multiprocessing system. 3 + 7 + 5

8. a) Consider the following sequence of instructions :

$I_1 : V_3 = V_1 \times V_2$

$I_2 : V_4 = V_3 + V_6$

$I_3 : V_0 = V_0 + V_7$

$I_4 : S_2 = V_1 \times S_3$

Why or why not, these instructions can be parallelized ?

b) What is multifunctional pipeline ?

c) Explain superscalar processor. 5 + 5 + 5

9. a)

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| S1 | × | | | | | | | | × |
| S2 | × | | | | | × | × | | |
| S3 | | | × | | | | | × | |
| S4 | | × | | | | | × | | |
| S5 | | | | × | × | | | | |

On the above reservation table calculate the distance set and forbidden list and also calculate the collision vector.

b) $C$ = 10110001. Draw the state diagram of the collision vector. 7 + 8

10. a) Suppose that the same program is executed on two different machines — $A$ and $B$. Compilers and data set on both the machines are identical. Given that :

| | |
|---|---|
| Machine $A$ | Average CPI = 3·5 |
| | Cycle time = 1·0 ns |
| Machine $B$ | Average CPI = 1·2 |
| | Cycle time = 0·5 ns |

Which out of those two machines is slower ? Justify your answer.

b) Time to complete $n$ task in a $k^{th}$ stage for non pipeline system = $nk$ ( unit delay of each stage ) and for pipeline system $k + ( n - 1 )$ clock cycle.

Is this statement true or false ? Justify your answer.

8 + 7

11. Write short notes on the following :

a) Data flow computers

b) VLIW processor architecture. 8 + 7