Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(AEIE)/SEM-1/EIEM-101/2012-13

2012

ADVANCED ELECTRONIC CIRCUITS

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* Questions.

All questions carry equal marks :

1. a) Find out the relationship between output current and reference current of a Widlar current source. 9

   b) Utilizing a reference current of 100 – μA, design a Widlar current source to provide an output current of 10 μA. Let the BJT have $V_{BE} = 0 \cdot 7$ V at 1-mA current assume β to be high. 5

2. a) Explain with the help of a diagram the operation of an active loaded MOS differential pair. 5

   b) Determine the transconductance G_m= and CMRR of the above MOS differential pair. 9

3. a) The BJT in the following circuit (Fig.-1) has V_{BE}=0·7 V β = 200 and V_A -100 V Find R0. 6

   b) Derive an expression for the output resistance of cascode MOS mirror. 8

4. a) What is a phase-locked loop ? Illustrate its working principle with the help of a simplified block diagram. 5

   b) Define loop locked range. Making use of detailed block diagram derive an expression for loop locked range. 9

5. a) What is propagation delay of a CMOS inverter? Derive an expression for t_{PHL} of an inverter. 9

   b) A CMOS inverter for which K_n= 10 K_p=100 μA/V^2, and $V_t = 0 \cdot 5$ V is connected to a sinusoidal signal source having Thevenin equivalent voltage of 0·1 V peak amplitude and resistance of 100 kΩ. What signal voltage appears at the output of the inverter with $V_1 = +1 \cdot 5$ V ? 5

6. a) Illustrate the use of hysteresis in the comparator characteristics as a means of rejecting interference. 7

   b) A bistable circuit is derived from a positive feedback loop by applying V_1 through R_1. Let $L+ = L- = 10$ V and R_1=1 kΩ. Find the value of R_2 that gives a hysteresis of 100mV width. 7

7. a) Explain giving suitable diagram the operation of a CMOS SRAM. 7

   b) Draw the relevant parts of the SRAM cell during a read operation. 7

8. a) Describe the operation of ECL 10k logic family as shown in Fig.-2. 9

   b) Calculate the value of V_R generated in the temperature and voltage compensated bias network in Fig.-2. 5

9. a) Obtain an expression for differential input resistance (R_{id}) of a general purpose 741 op-amp. If β_N of npn transistor is 200 and bias current is 9·5 μA, find the value of R_{id}. 8

   b) Also find the value of output resistance (Ro) of the 741 op-amp. 6

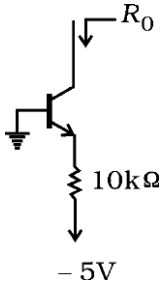

Fig.-1

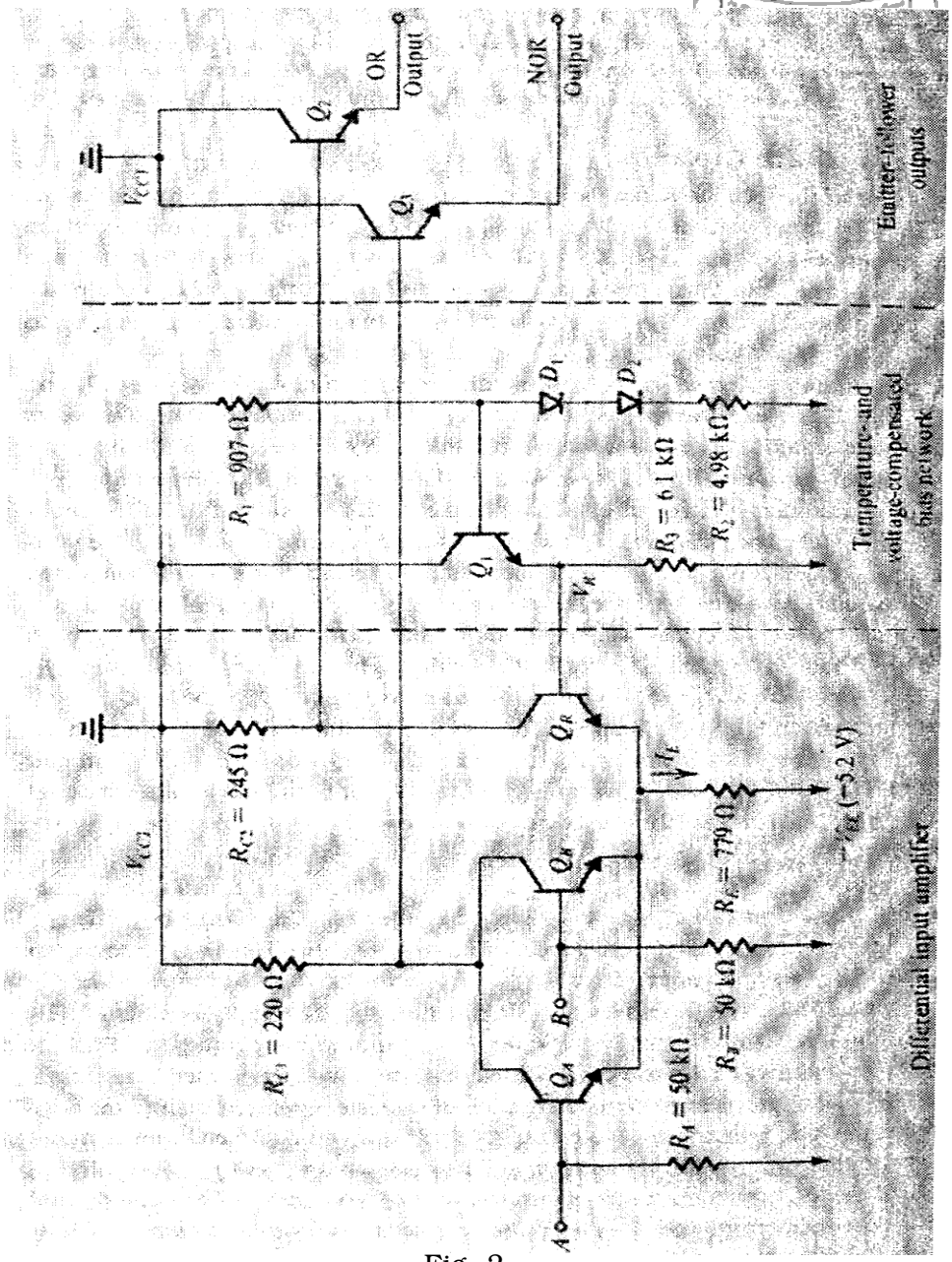
OR Output
NOR Output
V_{CC}
Q_2
Q_3
D_1
D_2
$R_1 = 907\ \Omega$
$R_2 = 4.98\ k\Omega$
$R_3 = 6.1\ k\Omega$
Q_1
V_M
Temperature- and voltage-compensated bias network
Emitter-follower outputs
Q_R
I_E
$-V_{EE}$ (−5.2 V)
$R_E = 779\ \Omega$
$R_{C1} = 245\ \Omega$
Q_B
$R_B = 30\ k\Omega$
$R_{C2} = 220\ \Omega$
B
Q_A
$R_A = 50\ k\Omega$
A
Differential input amplifier

Fig.-2