



Name :

Roll No. :

Invigilator's Signature :

CS/B.TECH(IT)/SEP.SUPPLE/SEM-8/IT-802C/2012

2012

VLSI DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

- i) What is the full form of FPGA ?
 - a) Field Programmable Gate Array
 - b) Full Programmable Gate Array
 - c) Fast Programmable Gate Array.
- ii) For a 2-input XOR gate what is the maximum number of MOS transistors ?
 - a) 16
 - b) 8
 - c) 6
 - d) 10.



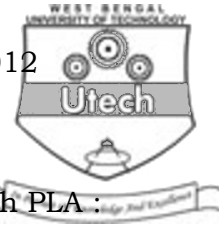
- viii) VLSI design flow is a
- a) cyclic process only
 - b) parallel process
 - c) sequential & cyclic process
 - d) none of these.
- ix) VHDL is a
- a) multi-threaded program
 - b) language like C
 - c) single user program
 - d) multi-user program.
- x) The output of physical design is
- a) circuit
 - b) layout
 - c) logical model
 - d) RTL schematic.
- xi) Typical manufacturing defects in IC fabrication are
- a) layer to layer shorts
 - b) discontinuous wires
 - c) missing or damaged vias
 - d) any of these.
- xii) Which of the following is not used in BIST ?
- a) PRBSG
 - b) ORA
 - c) BILBO
 - d) Tap controller.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Draw the layout of CMOS inverter.
3. Design half-adder with VHDL data flow modelling.



4. State & explain Kerninghan-Lin algorithm.
5. Implement the following Boolean function with PLA :
 - a) $Y = ab + bc + ca$
 - b) $F = ab' + abc'$.
6. What is FOX in IC fabrication ? Explain.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. Classify ASIC. Explain briefly the different ASIC.
8. What is Built in Self Test ? Explain with proper diagram.
9. Explain the *n*-well CMOS fabrication process with necessary diagram.
10. What do you understand by different stuck at faults ? What is the different technique to find them out ? Explain any one with proper example.
11. Write short notes on the following :
 - a) Need of testing
 - b) VHDL modelling of *D* flip-flop
 - c) Channel routing.

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