

Name :

Roll No. :

Invigilator's Signature :

CS/B.TECH(CSE/IT)-(OLD)/SEM-3/EC-312/2011-12

2011

DIGITAL ELECTRONICS AND LOGIC DESIGN

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

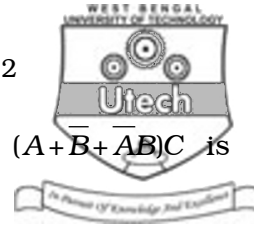
1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) What range of decimal values can be represented by a four-digit hexadecimal number ?

- | | |
|--------------|---------------|
| a) 0 to 1024 | b) 0 to 4096 |
| c) 0 to 8192 | d) 0 to 65535 |

ii) The OR operation can be produced with

- a) two NOR gates
- b) three NAND gates
- c) four NAND gates
- d) both (a) and (b).



iii) Simplified form of Boolean expression $(A + \overline{B} + \overline{A}B)C$ is

- a) 1
- b) 0
- c) C
- d) \overline{C} .

iv) A four-variable Karnaugh map has

- a) 8 min-terms
- b) 16 min-terms
- c) 32 min-terms
- d) 24 min-terms.

v) For an edge-triggered D flip-flop

- a) a change in the state of the flip-flop can occur only at a clock pulse edge
- b) the state that flip-flop goes to depend on the D input
- c) the output follows the input at each clock pulse
- d) all of these.

vi) A Full Adder can be constructed by using

- a) 2 AND gates, 3 XOR gates and an OR gates
- b) 3 AND gates, 2 XOR gates and an OR gates
- c) 3 AND gates, 2 XOR gates and 2 OR gates
- d) 2 AND gates, 2 XOR gates and 3 OR gates.



vii) A MOD-13 counter must have

- a) 13 flip-flops b) 3 flip-flops
- c) 4 flip-flops d) synchronous clocking.

viii) The fastest Logic family is

- a) TTL b) ECL
- c) IIL d) RTL.

ix) A unique operating feature of ECL circuit is its

- a) very high speed
- b) high power dissipation
- c) series base resistor
- d) compatibility with other logic families.

x) Which of the following devices selects one of the several inputs and transmits to a single output ?

- a) Decoder b) Multiplexer
- c) Demultiplexer d) Counter

xi) What is the NAND gate IC No. ?

- a) 7400 b) 7402
- c) 7404 d) none of these.

a) 8421 b) Excess-3

c) Gray d) ASCII.

(Short Answer Type Questions)

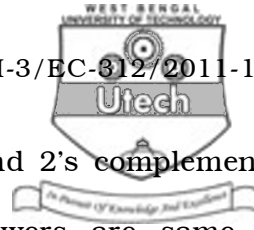
2. Implement a full adder circuit using decoder. 5

b) Minimize following expression using K-Map & realize the simplified expression using NAND gate only :

4. a) Why is Multiplexer called Data Selector ?

b) Implement the following expression using 8 : 1 Multiplexer :

$$F(A,B,C,D)=m(0,1,3,4,8,9,15) \quad 1 + 4$$



5. Do the following subtraction using 1's and 2's complement methods and show that both the answers are same :

$$(37)_{10} - (24)_{10}$$

$$2\frac{1}{2} + 2\frac{1}{2}$$

6. Design an Octal to Binary Encoder where all outputs are active high. 5

GROUP – C

(Long Answer Type Questions)

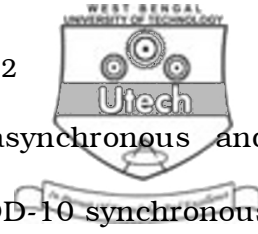
Answer any *three* of the following. $3 \times 15 = 45$

7. a) What is meant by duality of Boolean algebra ? Simplify the following Boolean algebra using K-map and realize the simplified function using NOR gates only.

$$F(A,B,C,D) = \Pi_M(1,2,3,8,10,11,14) + \sum_d(7,15)$$

- b) Construct a 5×32 decoder with four 3×8 decoders and a 2×4 decoder. Show block diagram only.

- c) Design a full-subtractor with two half subtractor and a logic gate. $(2 + 4 + 2) + 5 + 2$



8. a) What is the difference between asynchronous and synchronous counters ? Design a MOD-10 synchronous binary Up-counter using T flip-flops and other necessary logic gates.

b) What are the four basic types of shift register ? Draw the diagram of a 4-bit bi-directional shift register.

$$(2 + 7) + (2 + 4)$$

9. a) Design a 4-bit BCD to Excess-3 Converter circuit.

b) Design a 4-bit Full Adder circuit using Half Adders and OR gate.

c) What is Controlled Inverter ? 7 + 6 + 2

10. a) Implement the following expressions using PAL :

$$Y1 = ABC + AC$$

$$Y2 = ABC + AB$$



- b) Implement Ex-Or gate using NAND gate and NOR gate using NOR gate.
- c) What is prime implicant ? $7 + (3 + 3) + 2$
11. a) How do we convert J-K Flip-Flop to T Flip-Flop and J-K Flip-Flop to D Flip-Flop.
- b) Draw the circuit diagram of Master/Slave JK Flip-Flop and explain the operation of the circuit. $(5 + 5) + 5$
12. Write short notes on any three of the following : 3×5
- a) EEPROM
- b) Dual Slope ADC
- c) Parity Generator & Checker
- d) Parallel in Serial Out (PISO) shift register
- e) CMOS Logic.
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