Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech/EIE/SEM-8/EC-802A/2013

2013

DIGITAL SYSTEM DESIGN USING VHDL

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) VHDL is an acronym for

a) Very High Speed Integrated Circuits Hardware Description Language

b) Very High Definition Language

c) Very High Density Design Language

d) Versatile Hardware Description Language.

ii) Which of the following statements is correct ?

a) Signals can be declared within a process

b) Variables are local to a process

c) Process execution can be terminated

d) Signals can be assigned by a value instantaneously.

iii) Which of the following is a valid VHDL basic identifier ?

a) Last item b) Element#5

c) Entry d) All of these.

iv) VLSI design flow is a

a) cyclic process only

b) parallel process

c) sequential and cyclic process

d) all of these.

v) A process statement can be written without process if we use

a) if statement b) CASE statement

c) WAIT statement d) LOOP statement.

vi) Comments can be written in VHDL by the which following syntax

a) - b) --

c) /* d) */.

vii) Which of the following statements are correct ?

a) In a function all parameters are input parameters

b) In a procedure all parameters are input parameters

c) A function can have all types of parameters

d) Procedure does not have any parameter.

viii) In mixed style modeling

a) only behavioral modeling is allowed

b) only structural modeling is allowed

c) both behavioral and structural modeling is allowed

d) none of these is true.

ix) In VHDL Generic command is

a) local declaration

b) global declaration

c) both locally and globally

d) none of these.

x) SLA in VHDL is

a) Logical operator b) Shift operator

c) relational operator d) sign operator.

xi) VHDL codes are inherently

a) sequential b) concurrent

c) both (a) and (b) d) none of these.

xii) Which of the following language is used for hardware description ?

a) VHDL b) T-SPICE

c) LASI d) MATLAB.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Explain the differences in between signal and variable in the context of VHDL with an example.

3. Write a program to implement a J-K Flip-Flop in VHDL.

4. Briefly explain different types of operators available in VHDL with examples.

5. What do you mean by Hardware synthesis ? What are the constraints that affect the synthesis ? 2 + 3

6. Distinguish between top-down and bottom-up design methodologies for digital system.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Name the various languages to describe hardware.

b) What do you mean by “Entity”, “Architecture”, “Configuration” and “Package declaration” in a VHDL ?

c) Write a VHDL code in structural mode for Full Adder.

2 + 6 + 7

8. a) What do you mean by configuration in VHDL ?

   b) Give an example of default configuration, component configuration and architecture configuration.

   c) How generics can be used in configuration ? 3 + 9 + 3

9. a) Design a sequence detector to detect binary stream of '101' at input.

   b) What are the differences in a signal and a variable ? What is 'shared variable' ?

   c) What do you mean by deferred constant ? 8 + 5 + 2

10. a) Name the various types of subprograms available in VHDL language.

    b) Write down the differences in between function and procedure with suitable example.

    c) Write a VHDL code for 2-bit up-down counter. 3 + 7 + 5

11. a) What do you mean by package in VHDL ?

    b) Write down the two parts of package and briefly describe about them with an example.

    c) Write down the declaractions that can be declared in package.

    d) Write a package body in VHDL which contains subprogram declaration and constant declaration.

    2 + 6 + 3 + 4

12. Write short notes on any *three* of the following : 3 × 5

    a) Signal drivers

    b) VHDL library

    c) Moore type FSM

    d) Attributes in VHDL

    e) VHDL design flow and methodology.