Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech(EIE)/SEM-5/EI-502/2009-10

2009

MICROPROCESSOR BASED SYSTEM

Time Allotted : 3 Hours | Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) If ready pin is grounded, which states will introduce into the bus cycle of 8086/8088 microprocessor ?

   a) Idle b) Wait and remain idle

   c) Wait d) All of these.

   ii) The number of machine control flags in the flag register of 8086 microprocessor are

   a) 2 b) 3

   c) 4 d) 5.

   iii) Which one of the following is not a valid instruction ?

   a) XCHG AL, 01 [SI] b) MOV SI, 4000H

   c) MOV DS, 4000H d) STOSB.

iv) Mode 2 of 8254 is

a) bi-directional handshake mode

b) handshaking I/O

c) rate generator

d) square wave generator.

v) For a stepper motor, if the rotor teeth are equal to 200, the count required to rotate the shaft of the stepper motor through an angle 180° is

a) 200 b) 100

c) 50 d) 150.

vi) ADC chip 0808 is 8 bit CMOS, is

a) successive approximation type converter

b) dual-slope type converter

c) flash type converter

d) parallel converter.

vii) The NMI input is ..... - sensitive.

a) edge b) level

c) both edge and level d) none of these.

viii) The 8284A is a

a) clock generator b) bus controller

c) co-processor d) none of these.

ix) The 8288 I.C. is a/an

a) clock generator b) ADC

c) bus controller d) DAC.

x) BHE signal is used to enable the

a) even memory bank b) odd memory bank

c) both (a) and (b) d) none of these.

xi) If crystal oscillator frequency is operating at 24 MHz what will be the PCLK output of 8284A clock generator ?

a) 24 b) 8

c) 12 d) 6.

xii) In a μp the fetch / execute cycle is used to get and carryout which of the following ?

a) Data from memory

b) Data to memory

c) Instruction code

d) Demultiplexing multiplexed address / data bus.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) Define pipelining.

b) Discuss the function of instruction queue in 8086.

c) What is the maximum memory size that can be addressed by 8086 ? 1 + 3 + 1

3. a) Explain the different types of modes are used in 8237 controller.

   b) Describe the function of different bits of command register. 2 + 3

4. Select a SUB instruction that will :

   a) Subtract BX from CX

   b) Subtract OEEEH from DH

   c) Subtract DI from SI.

   Describe the functions of each bits of the command word register in the 8255. 2 + 3

5. How does 8086 support segmentation of memory ? What are the advantages of having segmentation ? 3 + 2

6. Write an assembly language program to find square root of a two digit number. Assume that the no. is a perfect square.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) What do you mean by addressing mode ? What are the different addressing modes supported by 8086 ? Explain each of them with suitable examples.

b) A single instruction may use more than one addressing mode or some instructions may not require any addressing mode. — Explain.

c) Draw and discuss in brief about the architecture of 8086 μp. (1 + 5) + 2 + 7

8. a) Explain with block diagram the sequence of events that occur when an IR line of 8259 connected to 8086 becomes high.

b) Design an 8086 based temperature measurement scheme using RTD as the sensor. Form a look-up-table for the above parameter and display the temperature on seven segment displays. 6 + 9

9. a) Interface an input port 74LS245 to read the status of switches SW1 to SW8 and an output port 74LS373 with 8086. Display the number of a key that is pressed *i.e.* from 1 to 8 on a 7-seg display with help of the output port. Write an ALP for this task, assume that only one key is pressed at a time. Draw the required hardware circuit. the i/p port address is 0008H and the o/p port address is 000AH.

b) What is the advantage of DMA control data transfer over interrupt driven or program controlled data transfer ?

c) Explain the following terms in relation to 8279 :

i) Two key lock-out

ii) N-key roll over. 8 + 3 + (2 + 2)

10. a) What do you mean by USART ? 2

b) Why USART is used ? 3

c) Design the hardware interface circuit for interfacing 8251 with 8086. Set the 8251 in asynchronous mode as a transmitter and receiver with even parity enabled, 2 stop bits, 8-bit character length, frequency is 160 kHz and baud rate 10 K. Write an ALP to —

i) transmit 100 bytes of data string stored from 2000 : 3000H.

ii) receive 100 bytes of data string and store it from 3000 : 4000H. 2 + 3 + 10

11. a) How can two 8259 be cascaded ?

b) What is the need of EOI command to 8259A and when do you use two commands ?

c) Draw and explain in brief the internal architecture of 8259A.

d) Describe the process of data transfer from the peripheral to the system memory under 8237 DMA controller. 2 + 2 + 6 + 5

12. Write short notes on any *three* of the following : 3 × 5

a) Read & write cycle of 8086

b) Interrupt sequence of 8086

c) 8279 (Programmable Keyboard / Display Controller)

d) Decoding techniques

e) Serial data transmission method.